Lab Note Book
lab1-9

Create by/Juddo Abaker

For Lab 6 My :Lab Partners for the Simulations and results were Jose Alberto Tapia

For Lab 6 My :Lab Partners for the Simulations and results were Steve Kepler and Jarry clark

For Lab (3,4,5,7,8,9) My :Lab Partners Steve Kepler for the Simulations and results

Logic Levels Lab 1

Lab 1 – Logic Levels

Names: ___Jose Alberto Tapia_____, ____ Juddo Abaker _____
Date: ____9/8/17_____

The purpose of this lab is to:
Learn how to create logic levels for digital circuits using switches and resistors.

Select four 10kohm resistors.
Measure and record the resistance of each resistor.

Equipment needed:

1 – Digital Multimeter
4 – 10Kohm
1 – 4 position dip switch

Using Multisim simulate Figure 1 for each voltage level and record in Table 1. Then build and test and measure each voltage level and record in Table 1

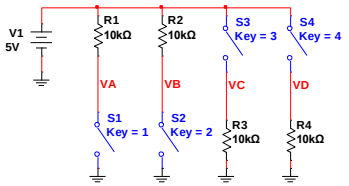


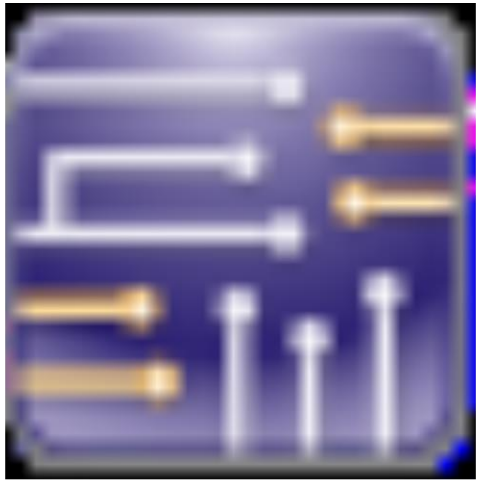
Figure 1- Lab 1 Schematic

	Simulated		Test	
	Open	Closed	Open	Closed
VA	5 V	0 V	5.03 V	0 V
VB	5 V	0 V	5.03 V	0 V
VC	0 V	5 V	0 V	5.03 V
VD	0 V	5 V	0 V	4.97 V

Table 1 (Simulation vs Test)

Observations:___Resistors: 10.016 K, 9.874 K, 9.701 K, 9.875 K.
_____We observed how in a simulated environment, the values tend to neglect any other variables that could affect the outcome. Meanwhile, in the lab we noticed how values tend to change with what the professor says is the result of variable such as friction or heat that tends to change the measured voltage coming from the resistors.
_____
_____
_____

Lecture2.ms14



Design1-lacture2.ms14

calculation

2	1	0	210
200	10	0	

calculation2.

2	1	0	210
200	10	0	
1	0	0	
4	2	1	
4	0	0	
			100

Lecture(2)a-11

lecture2a-11						
0	0	0	0	0000	0	0
0	0	0	1	0001	1	1
0	0	1	0	0010	2	2
0	0	1	1	0011	3	3
0	1	0	0	0100	4	4
0	1	0	1	0101	5	5
0	1	1	0	0110	6	6
0	1	1	1	0111	7	7
1	0	0	0	1000	8	8
1	0	0	1	1001	9	9
1	0	1	0	1010	10	A
1	0	1	1	1011	11	B
1	1	0	0	1100	12	C
1	1	0	1	1101	13	D
1	1	1	0	1110	14	E
1	1	1	1	1111	15	F

Lecture(1)silde(20)

2	1	0	210
200	10	0	
1	0	0	
4	2	1	
4	0	0	
			100

Lecture(1)slide(21)

8	4	2	1	Decimal value	Binary	Decimal	Octal	Hexadecimal
0	0	0	0	0	0000	0	00	00
0	0	0	1	1	0001	1	01	01
0	0	1	0	2	0010	2	02	02
0	0	1	1	3	0011	3	03	03
0	1	0	0	4	0100	4	04	04
0	1	0	1	5	0101	5	05	05
0	1	1	0	6	0110	6	06	06
0	1	1	1	7	0111	7	07	07
1	0	0	0	8	1000	8	10	08
1	0	0	1	9	1001	9	11	09
1	0	1	0	10	1010	10	12	0A
1	0	1	1	11	1011	11	13	0B
1	1	0	0	12	1100	12	14	0C
1	1	0	1	13	1101	13	15	0D
1	1	1	0	14	1110	14	16	0E
1	1	1	1	15	1111	15	17	0F

Lab(2)

Lecture(2)

lecture2a-1

1	0	0	1	1															
16	8	4	2	1															
16	0	0	2	1															
				19															

lecture 2a -2

1	1	0	1	1															
16	8	4	2	1															
16	8	0	2	1	27														
				11011=27															

lecture2a-3

1	0	1	1	0	1	0	1												
128	64	32	16	8	4	2	1												
128	0	32	16	0	4	0	1	181											
					10110101=181														

lecture2a-4

1	0	1	1	0	0														
32	0	8	4	0	1	45													

lecture2a-5

1	0	0	1	1	0	0													
64	0	0	8	4	0	0	76												

lecture2a-6

45	101101																		

lecture2a-7

76	1001100																		

Lecure2a(12)

lectuer2a-12		(HEX-DEC)		
848				
3	5	6		
256	16	1		
768	80	6	854	
			356	
848				
2	A	F		
2	10	15		
256	16	1		
512	160	15	687	
			2AF	
1	B	C	2	
	11	12	2	
	256	16	1	
		192	2	194
				C2

Lab(3) – Logic Gates

EECT112

Lab 3 – Logic Gates

Names: Steve Kepler Araker
Date: 9-29-17

The purpose of this lab is to:
Learn how to test AND and OR logic gates.

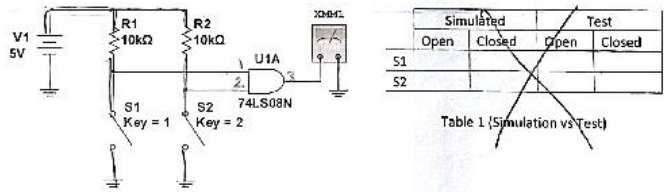
Select two 10kohm resistors.
Measure and record the resistance of each resistor.

Equipment needed:

1 – Digital Multimeter
2 – 10Kohm
1 – 4 position dip switch
1 – 74LS08
1 – 74LS32

S1	S2	SIM	LAB
CLOSE	CLOSE	0 V	0.16 V
CLOSE	OPEN	0 V	0.16 V
OPEN	CLOSE	0 V	0.16 V
OPEN	OPEN	5 V	4.38 V

Using Multisim simulate Figure 1 for each voltage level and record in Table 1. Then build, test and measure each voltage level and record in Table 1



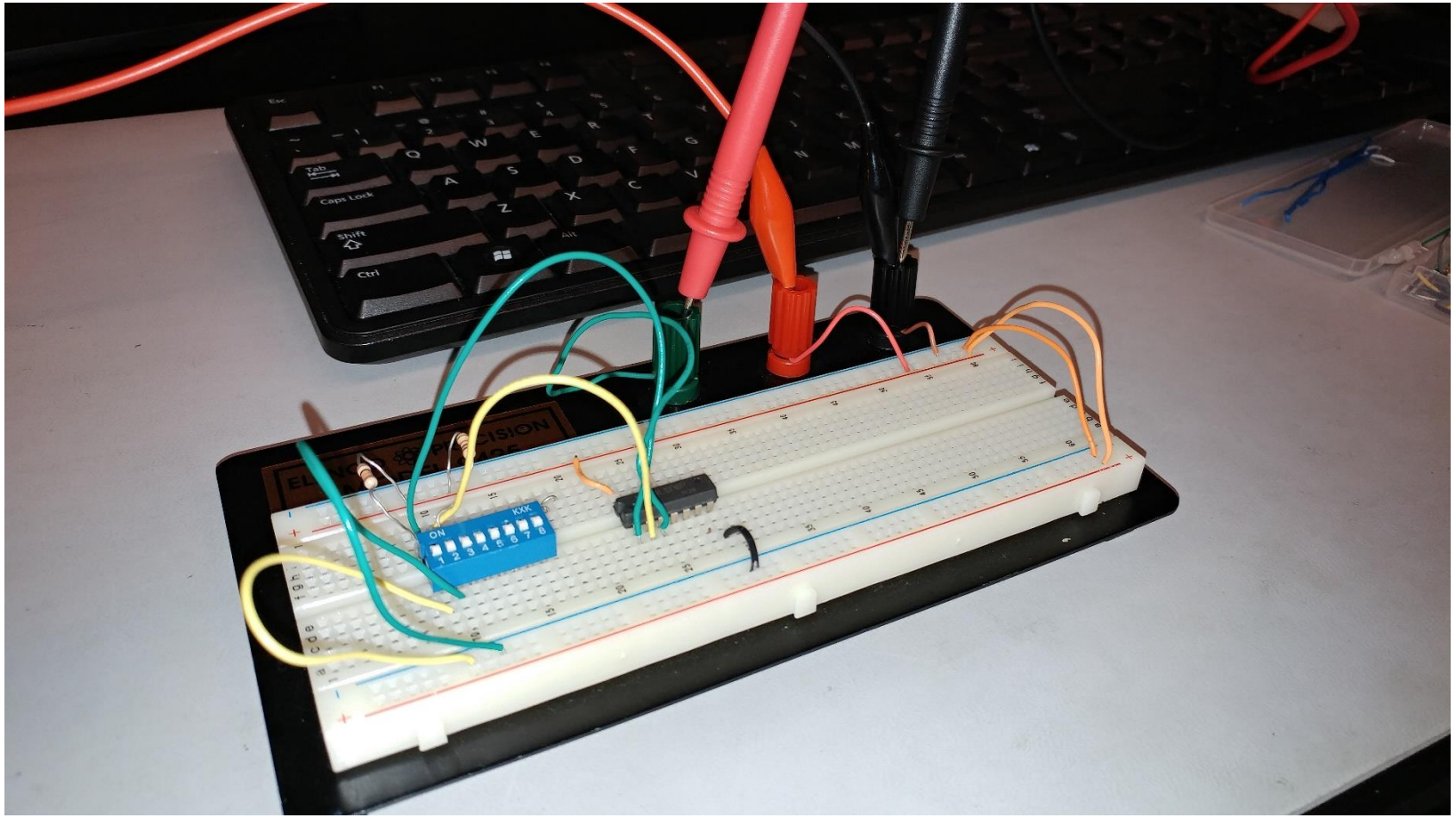
	Simulated		Test	
	Open	Closed	Open	Closed
S1				
S2				

Table 1 (Simulation vs Test)

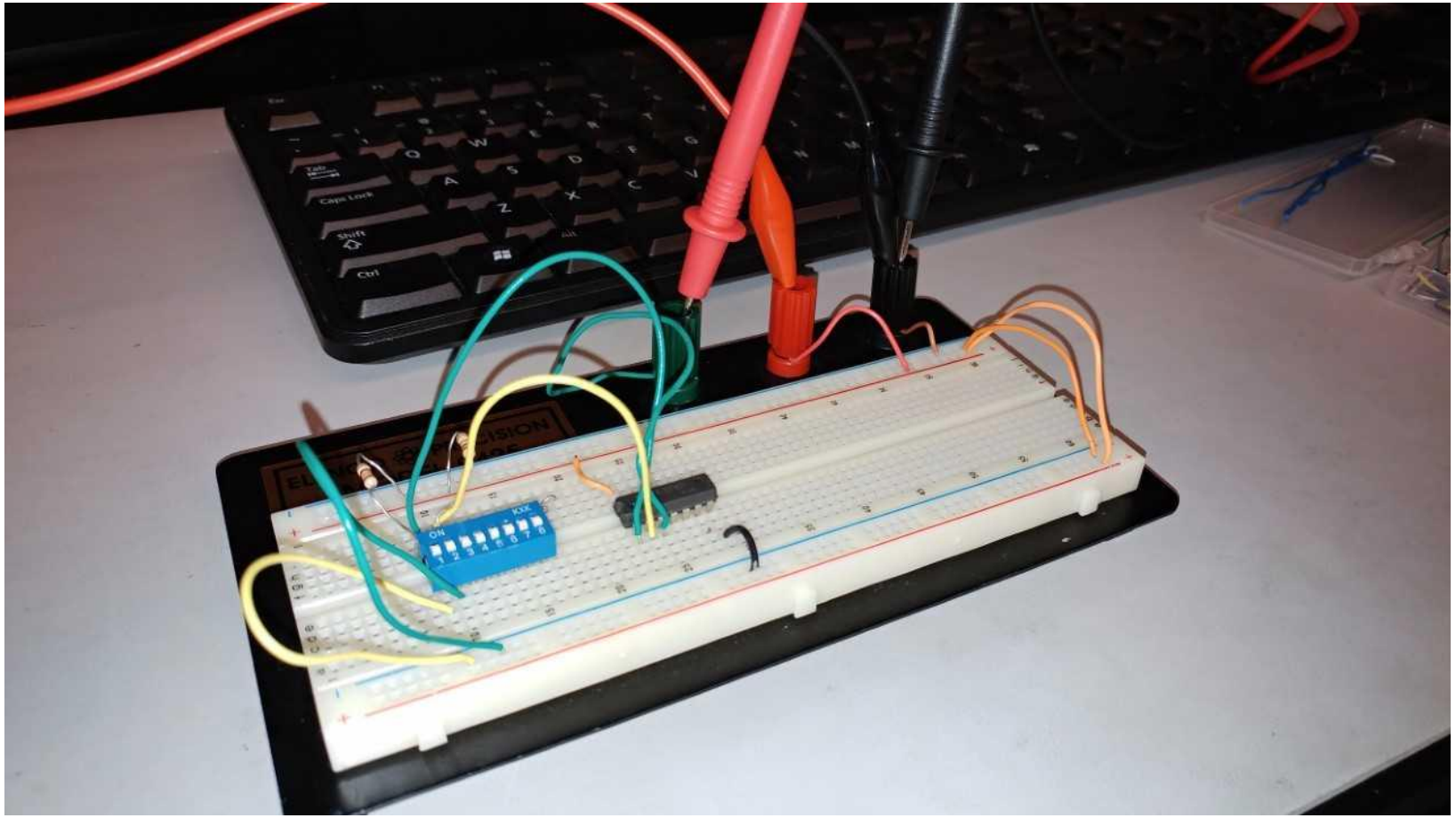
Figure 1- Lab 3 Schematic

Using Multisim simulate Figure 2 for each voltage level and record in Table 2. Then build, test and measure each voltage level and record in Table 2

Lab(3)-photo(1)



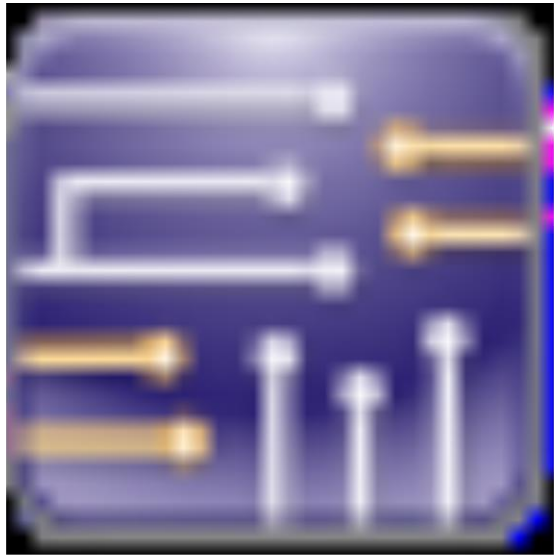
Lab(3)photo(2)



Gate1-6 calculation

ckt1 or Gate			ckt2 AND Gate			ckt3 NAND Gate			ckt4 Nor Gate				ckt5 XOR Gate				ckt6 X NOR Gate		
A	B	out	A	B	out	A	B	out	A	B	out		A	B	out		A	B	out
0	0	0	0	0	0	0	0	1	0	0	1		0	0	0		0	0	1
0	1	1	0	1	0	0	1	1	0	1	0		0	1	1		0	1	0
1	1	1	1	1	0	1	1	1	1	1	0		1	1	1		1	1	0
1	0	1	1	0	1	1	0	0	1	0	0		1	0	0		1	0	1

Gate(3)



Gate(3).ms14

Mid-T-lab6

Mid-T-part2

Lab(4)

EECT112 – 50C

Lab 4 – Lecture 3b Slide 3

Names: Judd Abaky Steve Keppen
Date: 10/6/17

The purpose of this lab is to:
Learn more about describing Logic Circuits algebraically.

Select three 10kohm resistors.
Measure and record the resistance of each resistor.

$V = IR$
$0 = (0)(10k)$
$I = \frac{V}{R} = \frac{5}{10,000}$
$= .5mA$

Equipment needed:

1 – Digital Multimeter
3 – 10Kohm
1 – 4 position dip switch
1 – 74LS08
1 – 74LS32

Using Multisim simulate Figure 1 for each voltage level and record in Table 1. Then build, test and measure each voltage level and record in Table 1

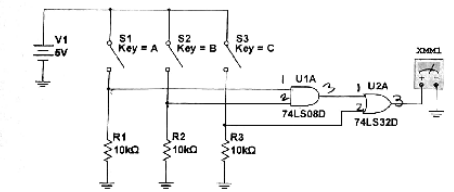


Figure 1- Lab 4 Schematic

	Simulated		Test	
	Open	Closed	Open	Closed
S1				
S2				
S3				

Table 1 (Simulation vs Test)

S1	S2	S3	SIM OUT	LAB OUT
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

Mid-T-part3

Lab(4)-test

S1	S2	S3	1*2	(1*2)+3	
0	0	0	0	0	FALSE
0	0	1	0	1	TRUE
0	1	0	0	0	FALSE
0	1	1	0	1	TRUE
1	0	0	0	0	FALSE
1	0	1	0	1	TRUE
1	1	0	1	1	TRUE
1	1	1	1	1	TRUE

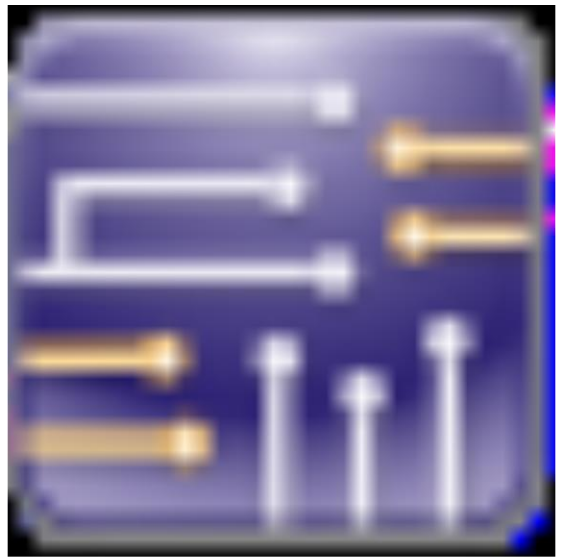
S1	S2	S3	1+2	(1+2)*3	
0	0	0	0	0	FALSE
0	0	1	0	0	FALSE
0	1	0	1	0	FALSE
0	1	1	1	1	TRUE
1	0	0	1	0	FALSE
1	0	1	1	1	TRUE
1	1	0	1	0	FALSE
1	1	1	1	1	TRUE

Mid-T-part5

Lecture-b4

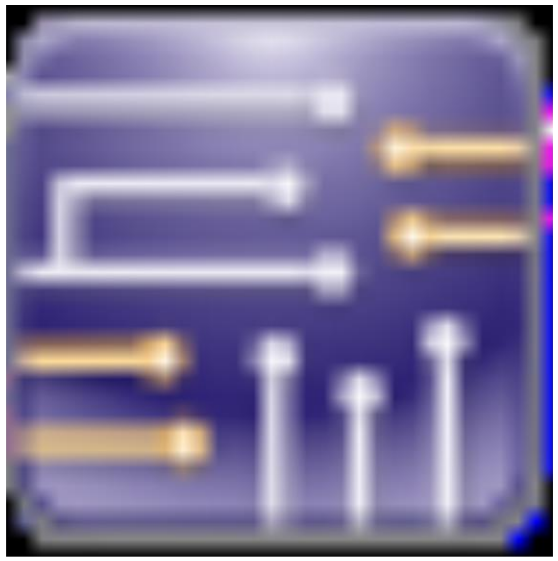
A	B	X							B'	B									
0	0	1	A'B'					A'	1	0									
0	1	0						A	0	1									
1	0	0		[X=A'B'+AB]															
1	1	1	AB																

A	B	C	D	X						C'D'	C'D	CD	CD'						
0	0	0	0	0					A'B'	0	1	0	0						
0	0	0	1	1					A'B'	0	1	0	0						
0	0	1	0	0	A'B'C'D				AB	0	1	1	0						
0	0	1	1	0					AB'	0	0	0	0						
0	1	0	0	0															
0	1	0	1	1															
0	1	1	0	0	A'BC'D	[X=A'B'C'D+A'BC'D+ABC'D+ABCD]													
0	1	1	1	0															
1	0	0	0	0															
1	0	0	1	0															
1	0	1	0	0															
1	0	1	1	0															
1	1	0	0	0															
1	1	0	1	1	ABC'D														
1	1	1	0	0															
1	1	1	1	1	ABCD														



Midterm.ms14

Mid-2



Midterm2.ms14

lab5

lab7

Lab-(7).pdf

Lab 7 – Circuit Reduction (Part 1

Lab 7 – Circuit Reduction (Part 1)

Names: Brett Barnett, Steve Kepler, Judd Abaker
Date: 27 October 2017

The purpose of this lab is to:
Learn how to reduce a circuit design down to the smallest size using the 17 Theorems and Karnaugh maps. Part 2 will explore how to reduce the circuit.

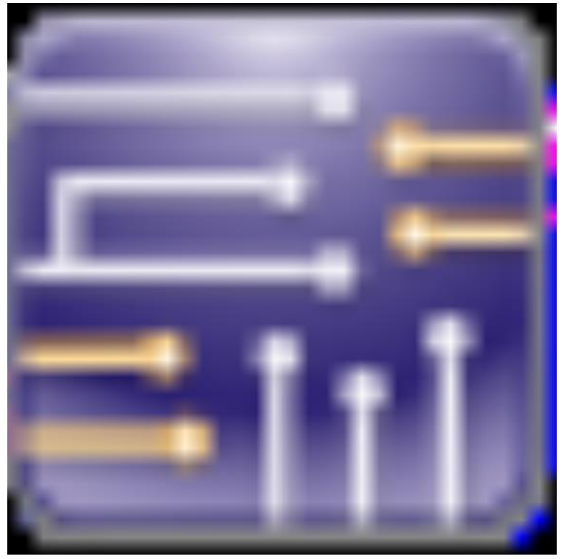
Select two 10kohm resistors.
Measure and record the resistance of each resistor.

Equipment needed:

1 – Digital Multimeter
3 – 10Kohm
1 – 4 position dip switch
1 – 74LS04 Hex Inverter
1 – 74LS00 Quad NAND
1 – 74LS11 Triple 3 input AND
1 – 74LS32 Quad OR

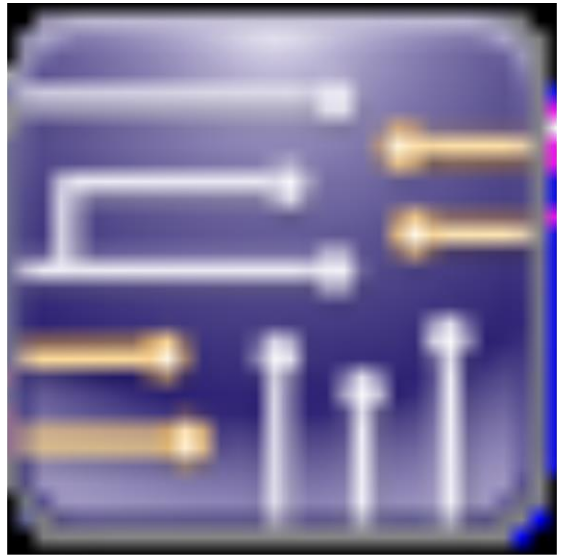
Using Multisim simulate Figure 1 for each input and record in Table 1. Then build and test circuit and record in Table 1

Lecture(4)slide3



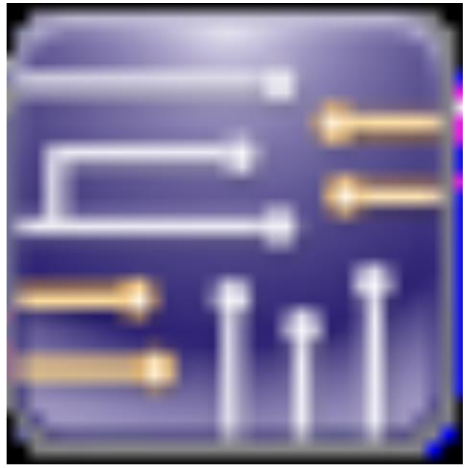
4-3.ms14

Lecture(4)slide4



4-4.ms14

Lecture(4)slide5

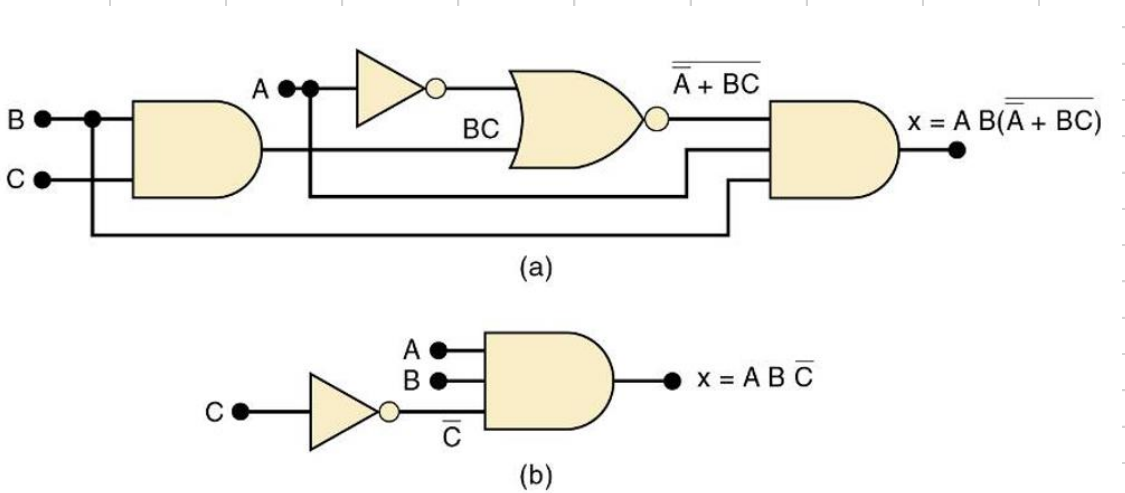


Lecture 4 - Slide 5.ms14

Lecture(4)slide(5)

leture (4) slide(5)

A	B	C	Output 1	Output 2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	1	1
1	1	1	0	0



Lab 8 – Circuit Reduction (Part 2)

Lab 8 – Circuit Reduction (Part 2)

Names: Juddo Abaker, Brett Barnett, Steve Kepler
Date: 10 November 2017

The purpose of this lab is to:
Learn how to reduce a circuit design down to the smallest size using the 17 Theorems and Karnaugh maps. Part 2 will explore how to reduce the circuit. You will also need the results of Lab 7.

Select three 10kohm resistors.
Measure and record the resistance of each resistor.

Equipment needed:

1 – Digital Multimeter
3 – 10Kohm
1 – 4 position dip switch
1 – 74LS04 Hex Inverter
1 – 74LS08 Quad AND
1 – 74LS32 Quad OR

Using Multisim simulate Figure 1 for each input and record in Table 1. Then build and test circuit and record in Table 1

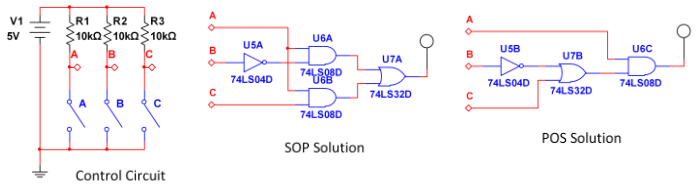
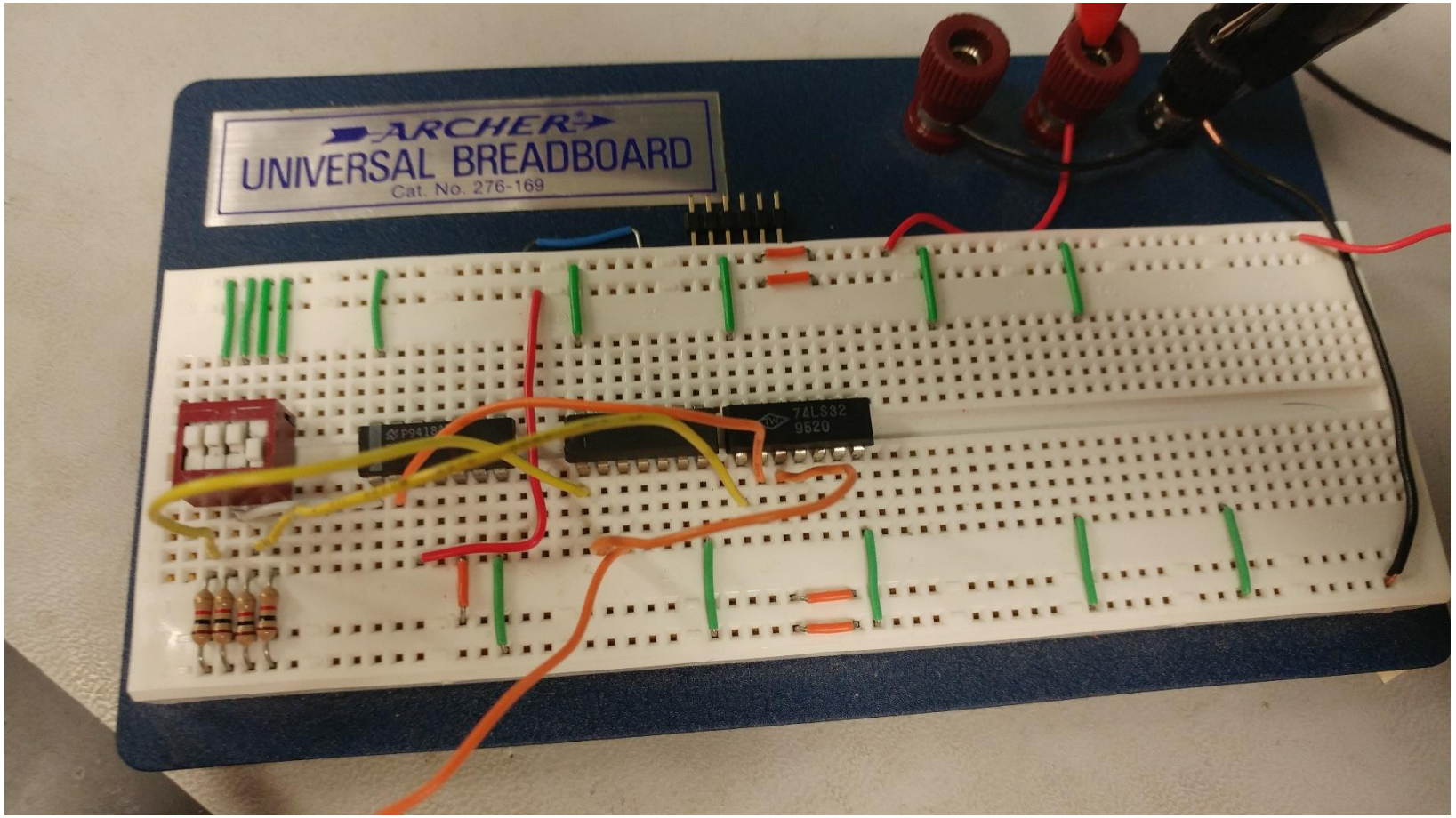


Figure 1- Lab 8 Schematic

lecure4b

A	B	X							B'	B									
0	0	1	A'B'					A'	1	0									
0	1	0						A	0	1									
1	0	0		[X=A'B'+AB]															
1	1	1	AB																

A	B	C	D	X						C'D'	C'D	CD	CD'						
0	0	0	0	0					A'B'	0	1	0	0						
0	0	0	1	1					A'B'	0	1	0	0						
0	0	1	0	0	A'B'C'D				AB	0	1	1	0						
0	0	1	1	0					AB'	0	0	0	0						
0	1	0	0	0															
0	1	0	1	1															
0	1	1	0	0	A'BC'D	[X=A'B'C'D+A'BC'D+ABC'D+ABCD]													
0	1	1	1	0															
1	0	0	0	0															
1	0	0	1	0															
1	0	1	0	0															
1	0	1	1	0															
1	1	0	0	0															
1	1	0	1	1	ABC'D														
1	1	1	0	0															
1	1	1	1	1	ABCD														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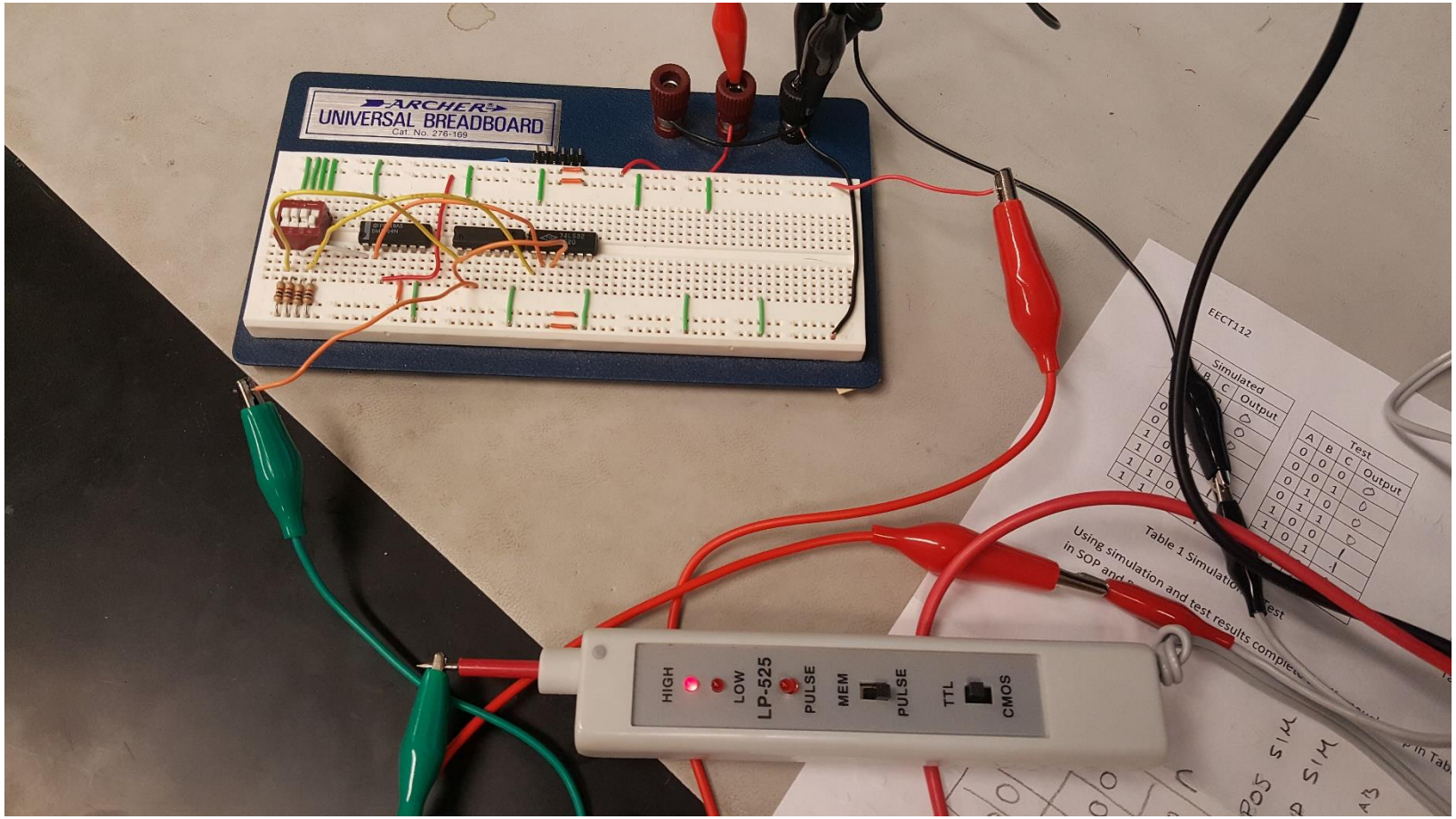
Cat. No. 276-169
74LS32
9620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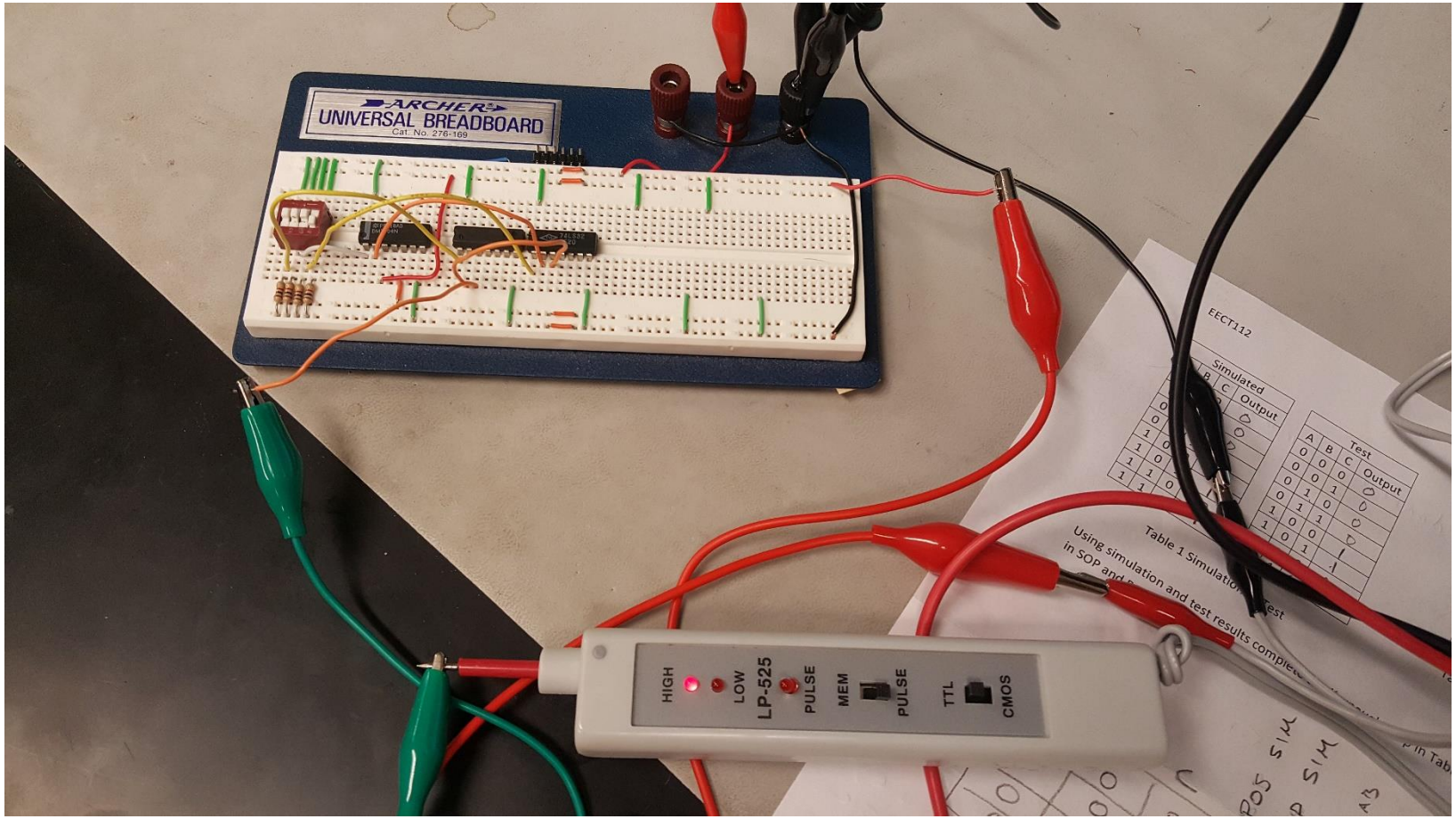
UNIVERSAL BREADBOARD
Cat. No. 276-169
HIGH
LOW
LP-525
PULSE
MEM
PULSE
TTL
CMOS
EECT112
Simulated
Test
Output
Table 1 Simulation
Using simulation and test results


ARCHER
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HIGH
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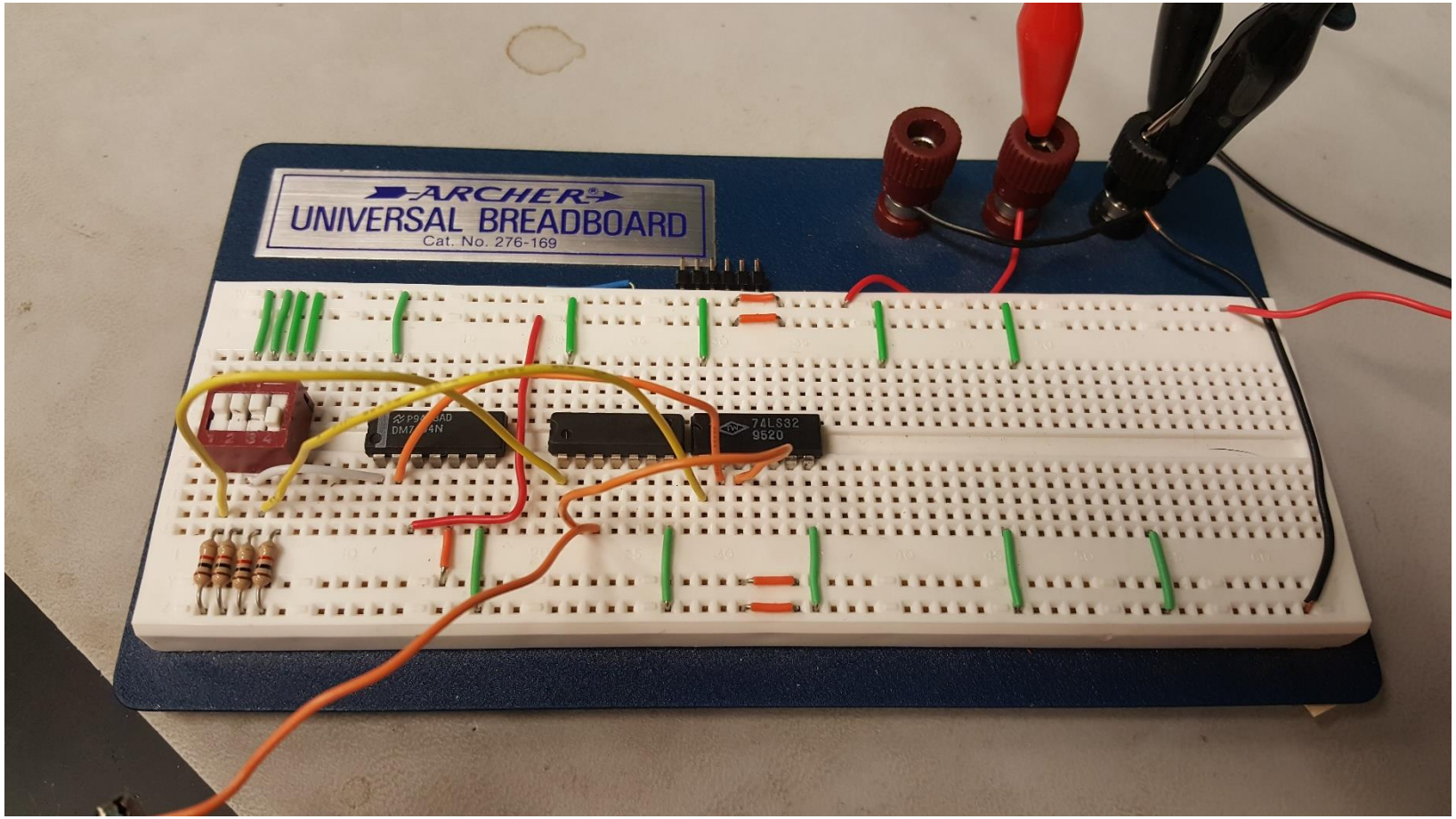
CMOS
EECT112
Simulated
Test
Output
Table 1 Simulation
Using simulation and test results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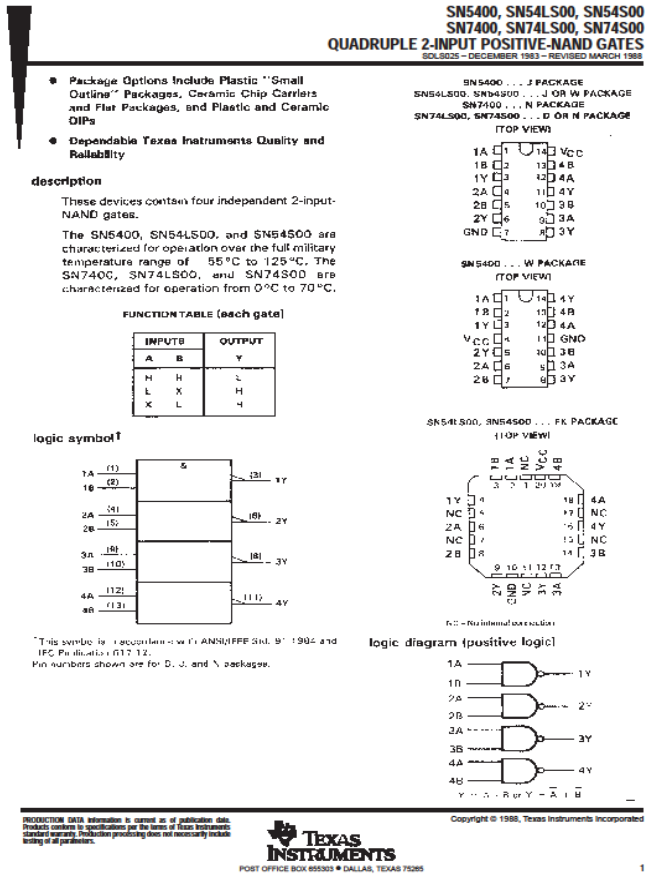
Cat. No. 276-169
74LS82
9520

Datasheets for all Parts used in this Lab Notebook



SN5400, SN54LS00, SN54S00
SN7400, SN74LS00, SN74S00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES
SDLS025 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input NAND gates.

The SN5400, SN54LS00, and SN54S00 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7400, SN74LS00, and SN74S00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

logic diagram (positive logic)

† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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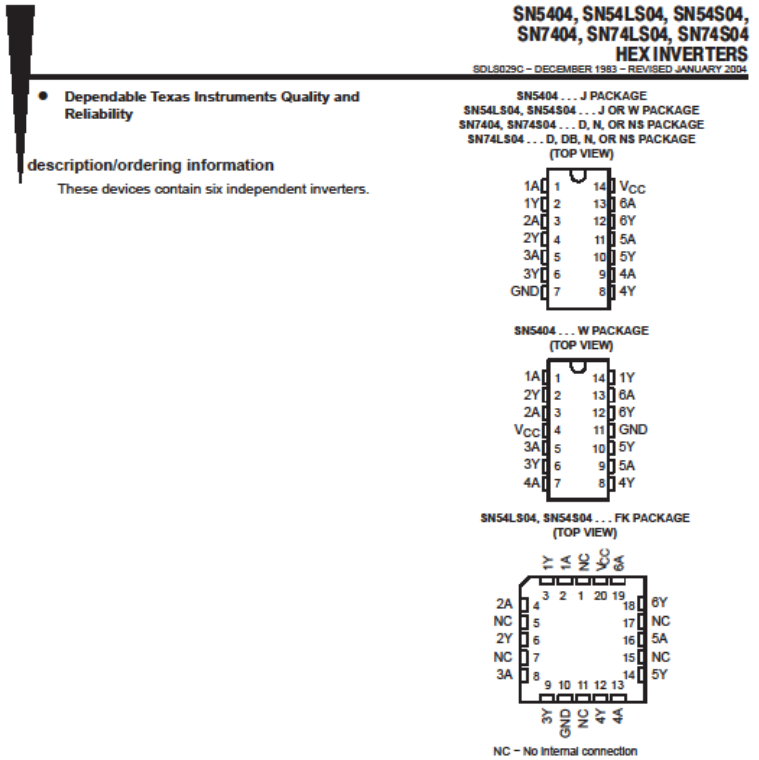

SN5404, SN54LS04, SN54S04,
SN7404, SN74LS04, SN74S04
HEX INVERTERS
SDLS029C – DECEMBER 1983 – REVISED JANUARY 2004

- Dependable Texas Instruments Quality and Reliability

description/ordering information

These devices contain six independent inverters.

NC – No internal connection

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Font Paragraph Styles

Normal No Spac... Heading 1 Heading 2 Title Subtitle Subtle Em... Emphasis Intense E... Strong

The purpose of this lab is to:

Learn how to reduce a circuit design down to the smallest size using the 17 Theorems and Karnaugh maps. Part 2 will explore how to reduce the circuit. You will also need the results of Lab 7.

Select three 10kohm resistors.
Measure and record the resistance of each resistor.

Equipment needed:

1 – Digital Multimeter
3 – 10Kohm
1 – 4 position dip switch
1 – 74LS04 Hex Inverter
1 – 74LS08 Quad AND
1 – 74LS32 Quad OR

Using Multisim simulate Figure 1 for each input and record in Table 1. Then build and test circuit and record in Table 1

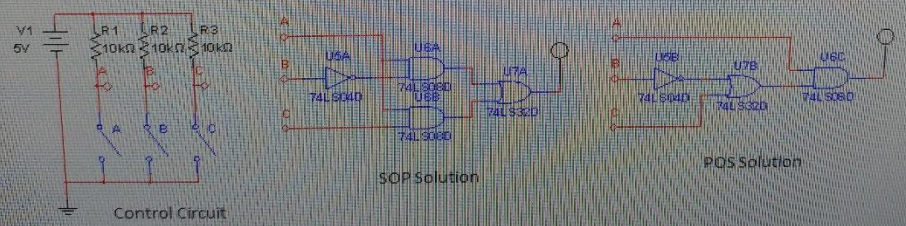
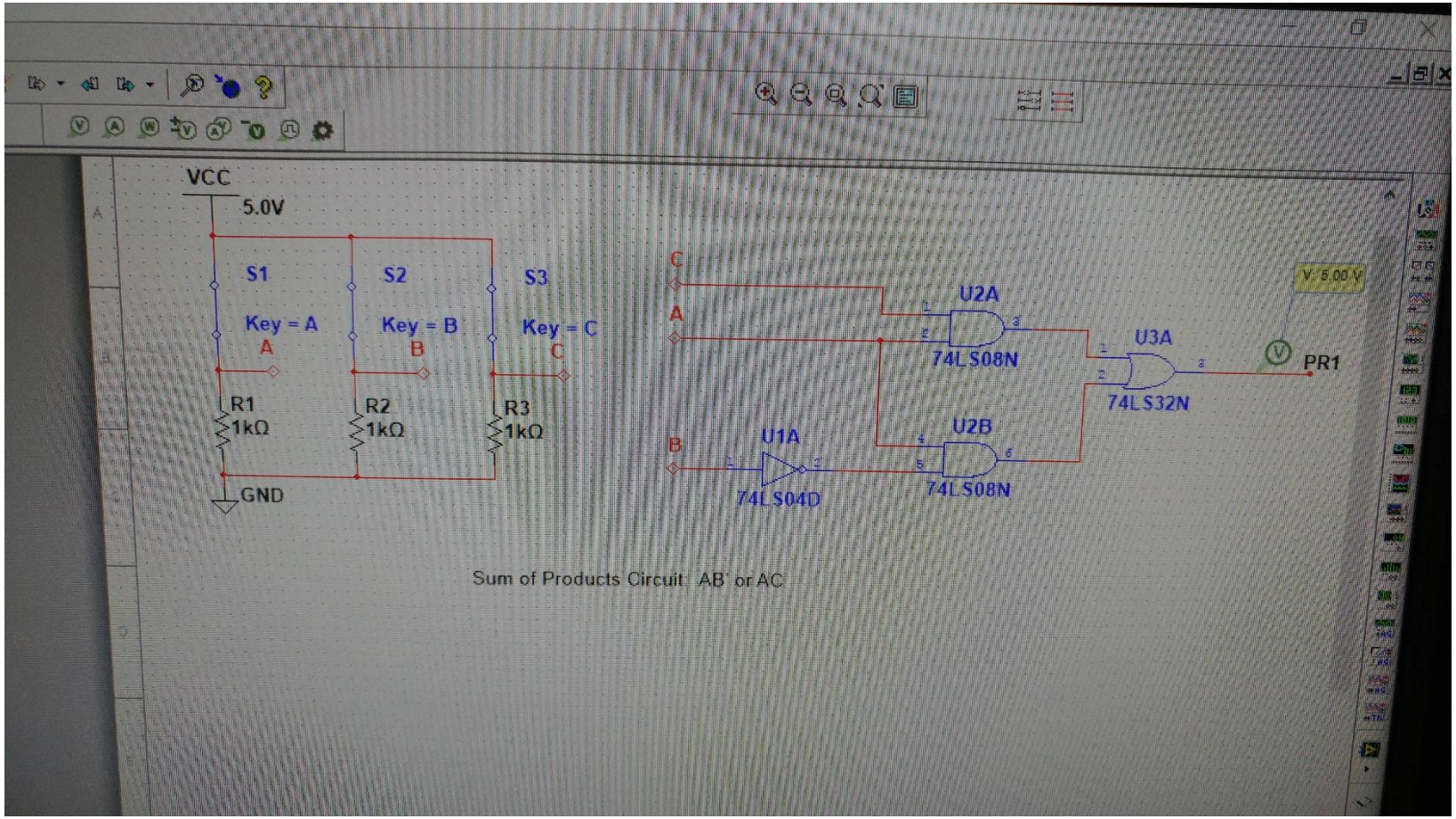
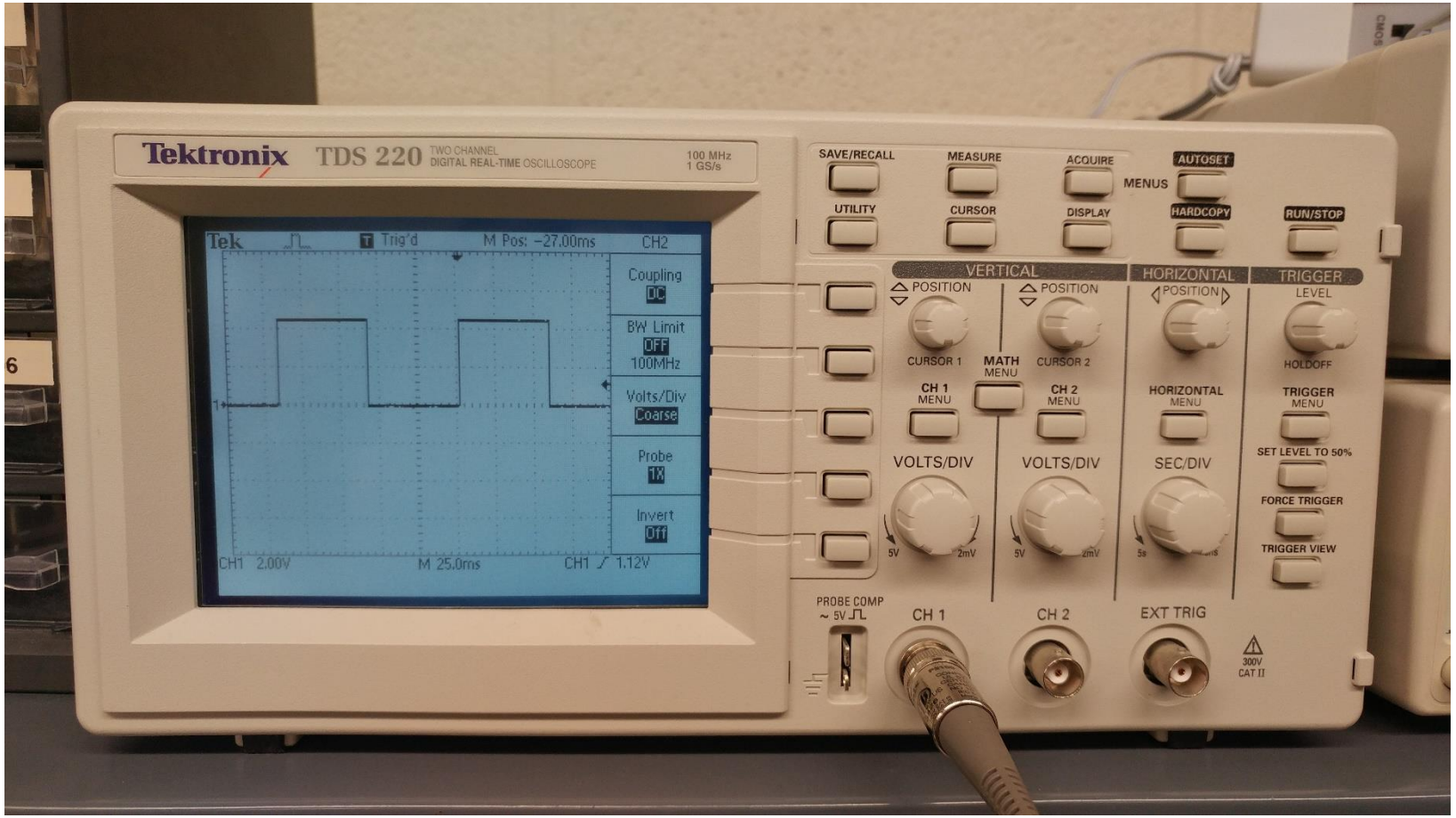


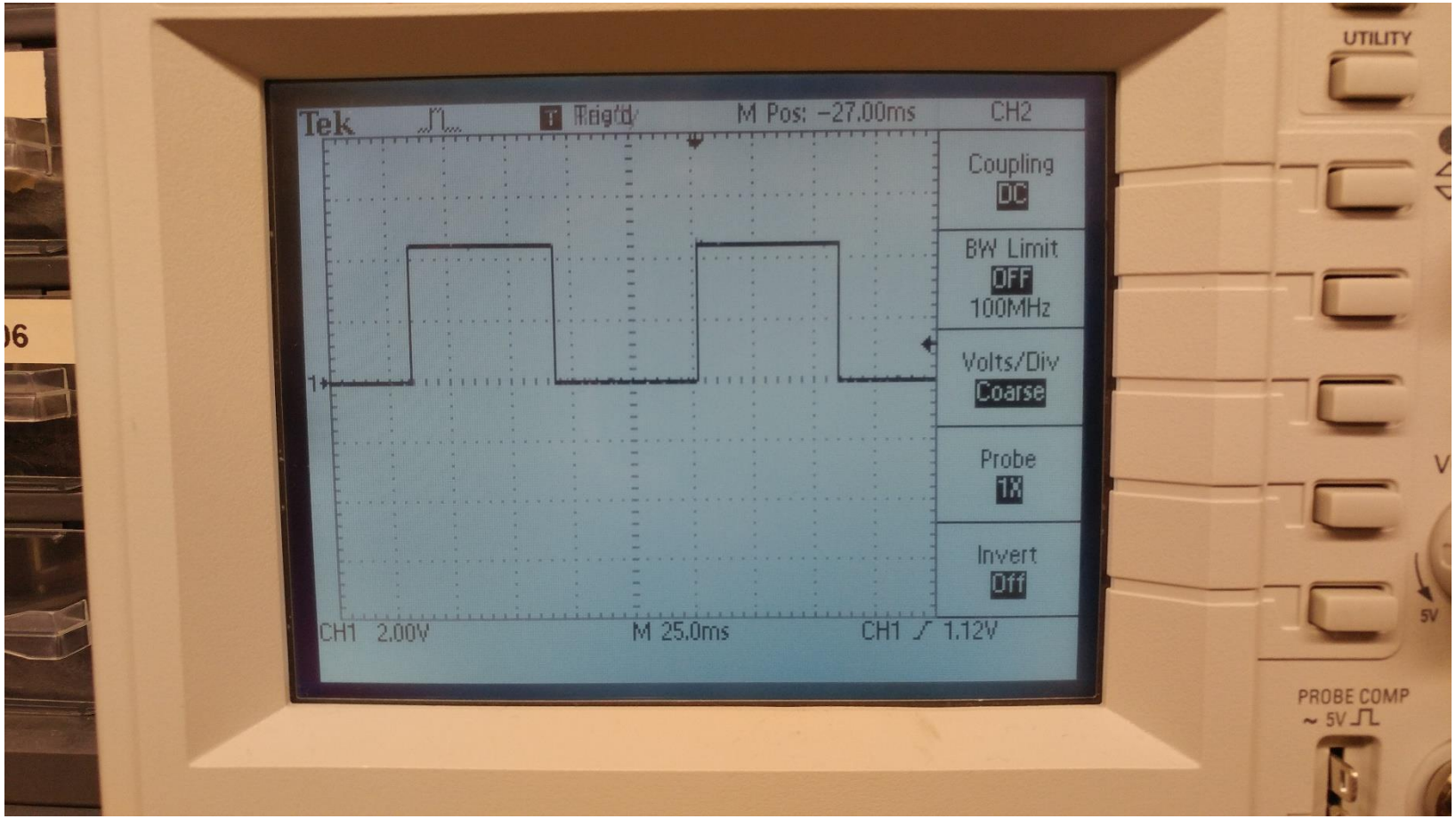
Figure 1- Lab 8 Schematic

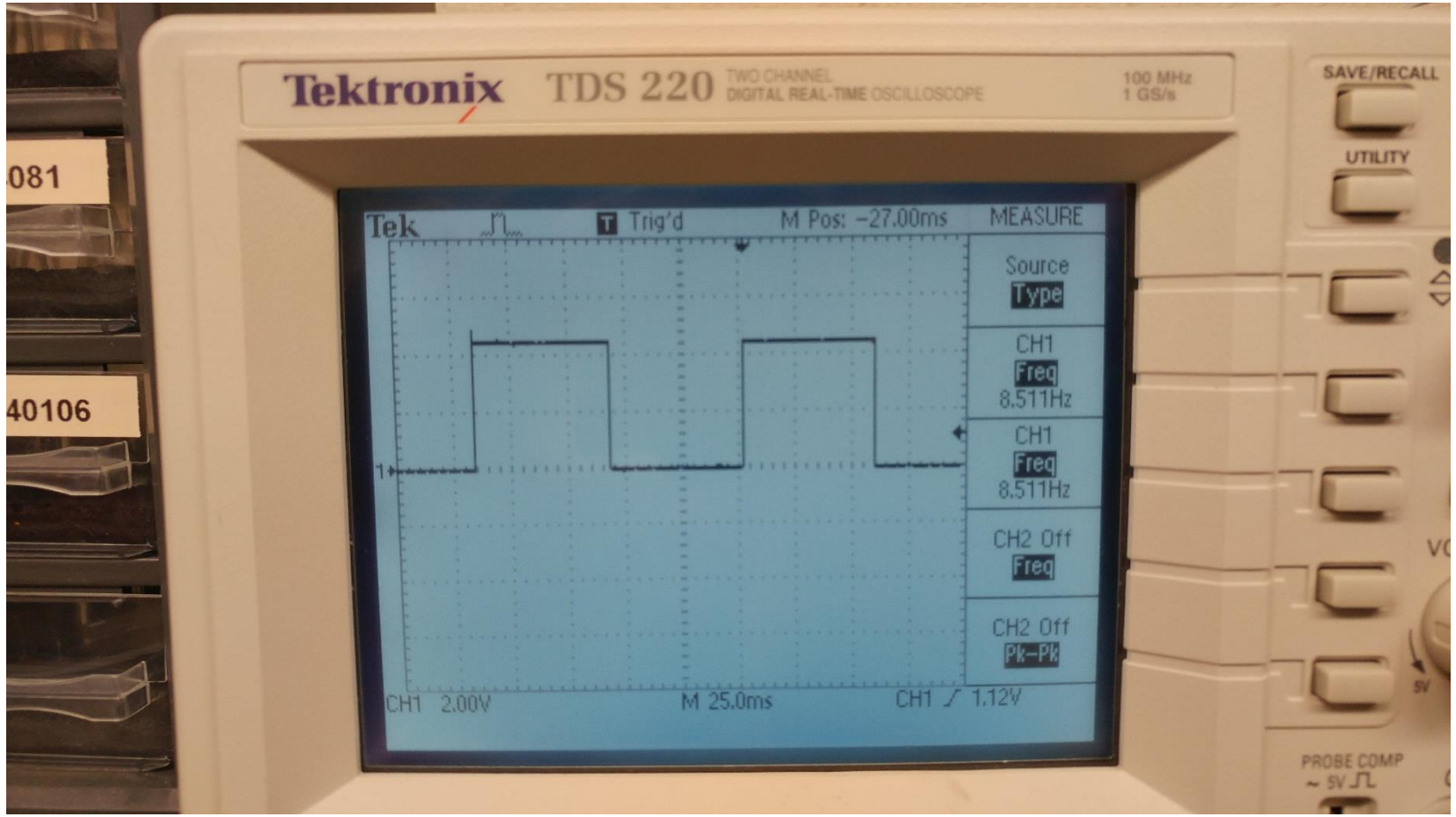

VCC
5.0V
S1
S2
S3
Key = A
A
Key = B
B
Key = C
C
R1
1kΩ
R2
1kΩ
R3
1kΩ
GND
C
A
B
U1A
74LS04D
U2A
74LS08N
U2B
74LS08N
U3A
74LS32N
V: 5.00 V
PR1
Sum of Products Circuit: AB' or AC

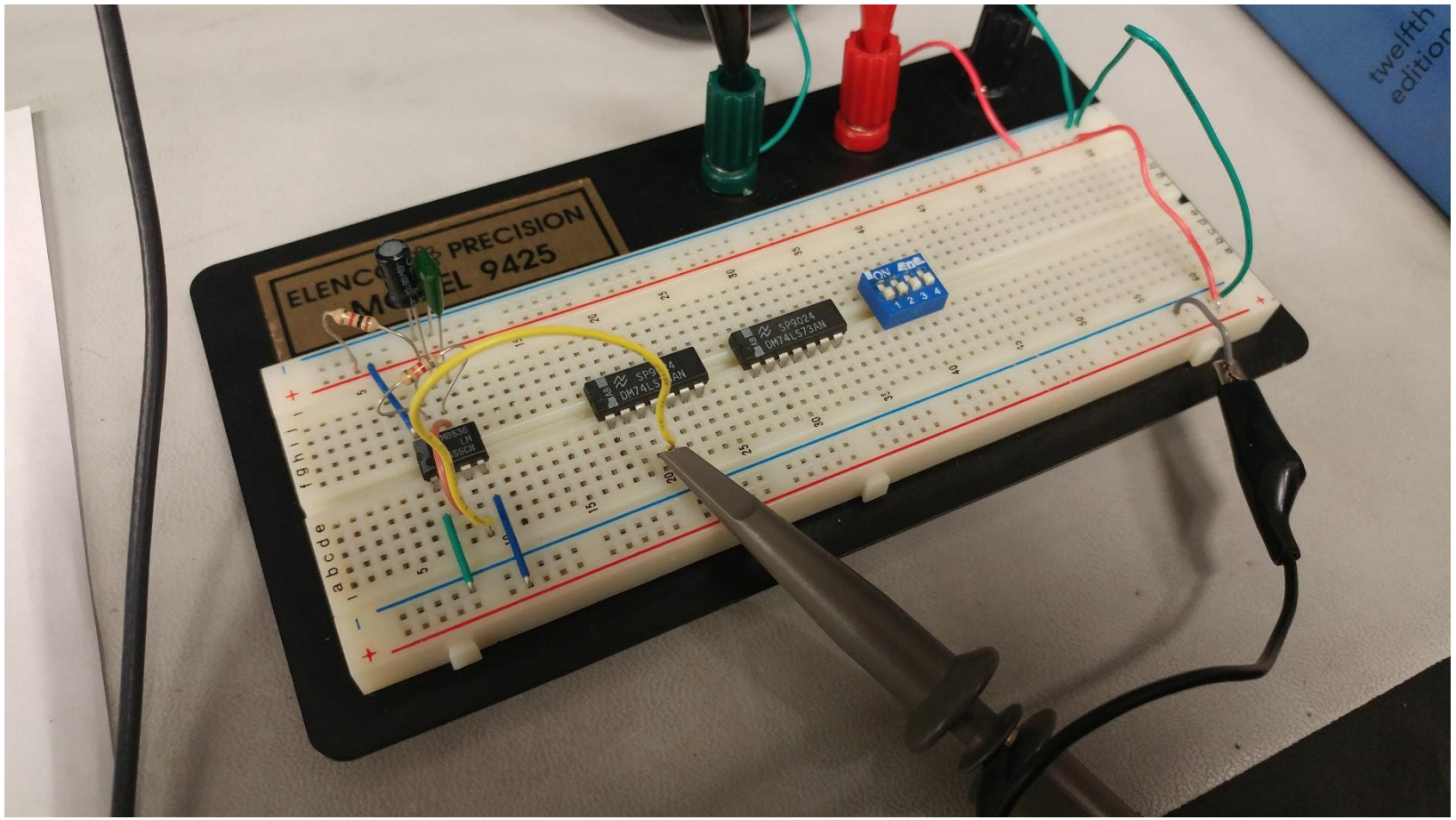
Lab9-1to 3 clock using JK Flops and 555 Timer

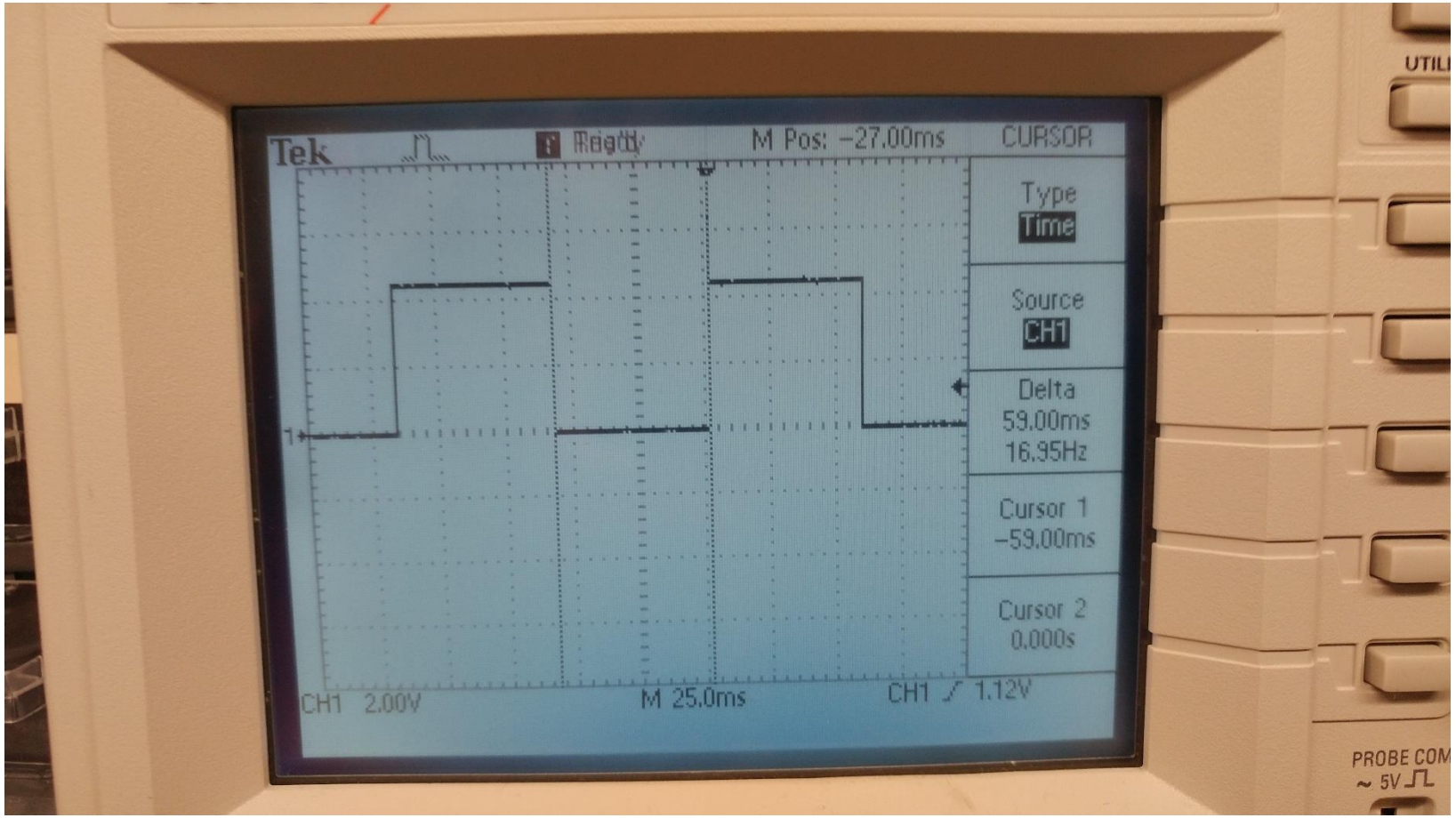
Lab(9)-A-B.pdf

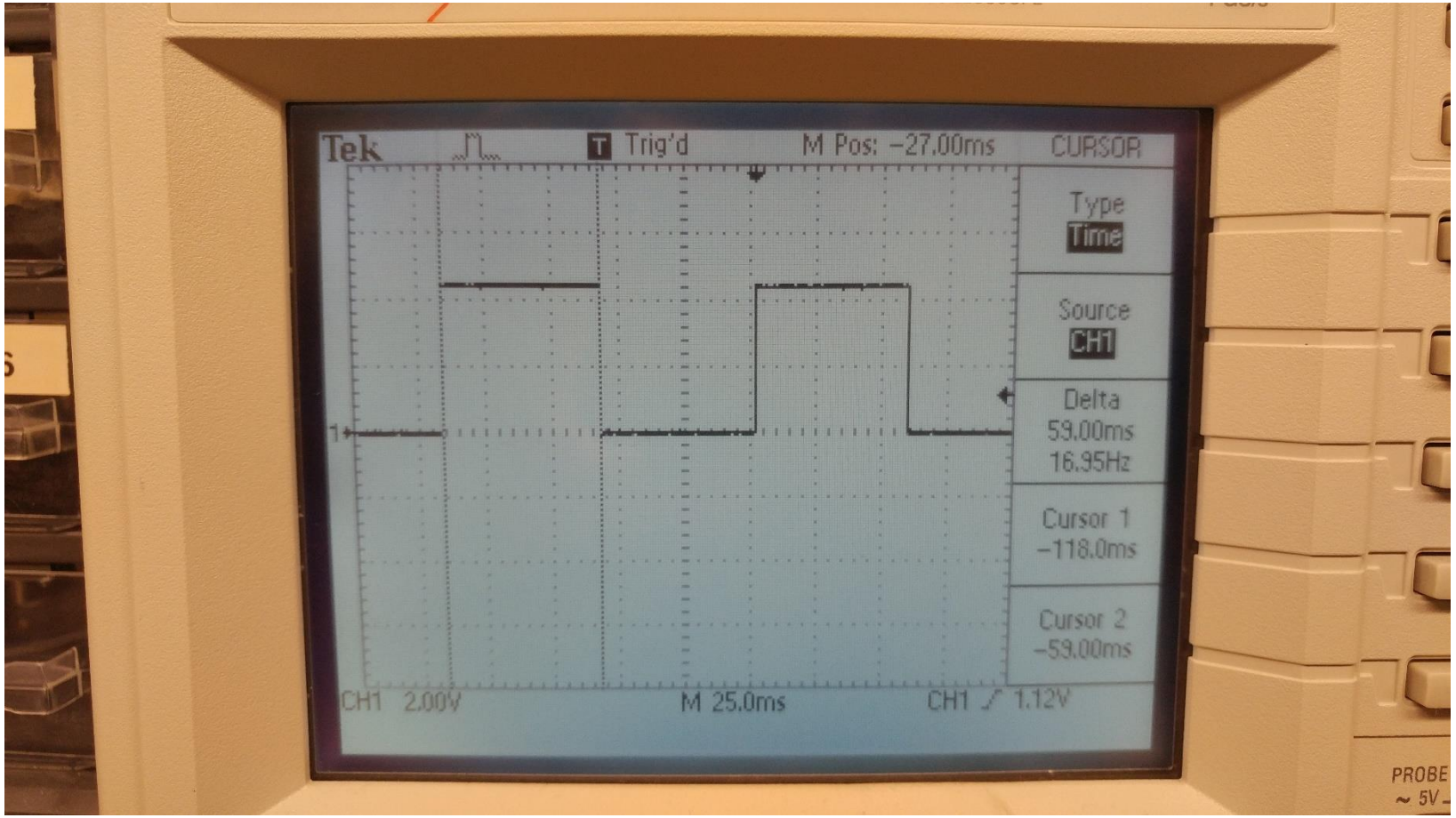

Tektronix
TDS 220
TWO CHANNEL
DIGITAL REAL-TIME OSCILLOSCOPE
100 MHz
1 GS/s
Tek
Trig'd
M Pos: -27.00ms
CH2
Coupling
DC
BW Limit
OFF
100MHz
Volts/Div
Coarse
Probe
1X
Invert
Off
CH1 2.00V
M 25.0ms
CH1 1.12V
SAVE/RECALL
MEASURE
ACQUIRE
AUTOSET
MENUS
UTILITY
CURSOR
DISPLAY
HARDCOPY
RUN/STOP
VERTICAL
HORIZONTAL
TRIGGER
POSITION
POSITION
POSITION
LEVEL
CURSOR 1
MATH
MENU
CURSOR 2
HOLDOFF
CH 1
MENU
CH 2
MENU
HORIZONTAL
MENU
TRIGGER
MENU
SET LEVEL TO 50%
VOLTS/DIV
VOLTS/DIV
SEC/DIV
FORCE TRIGGER
TRIGGER VIEW
5V
2mV
5V
2mV
5s
PROBE COMP
~ 5V
CH 1
CH 2
EXT TRIG
300V
CAT II

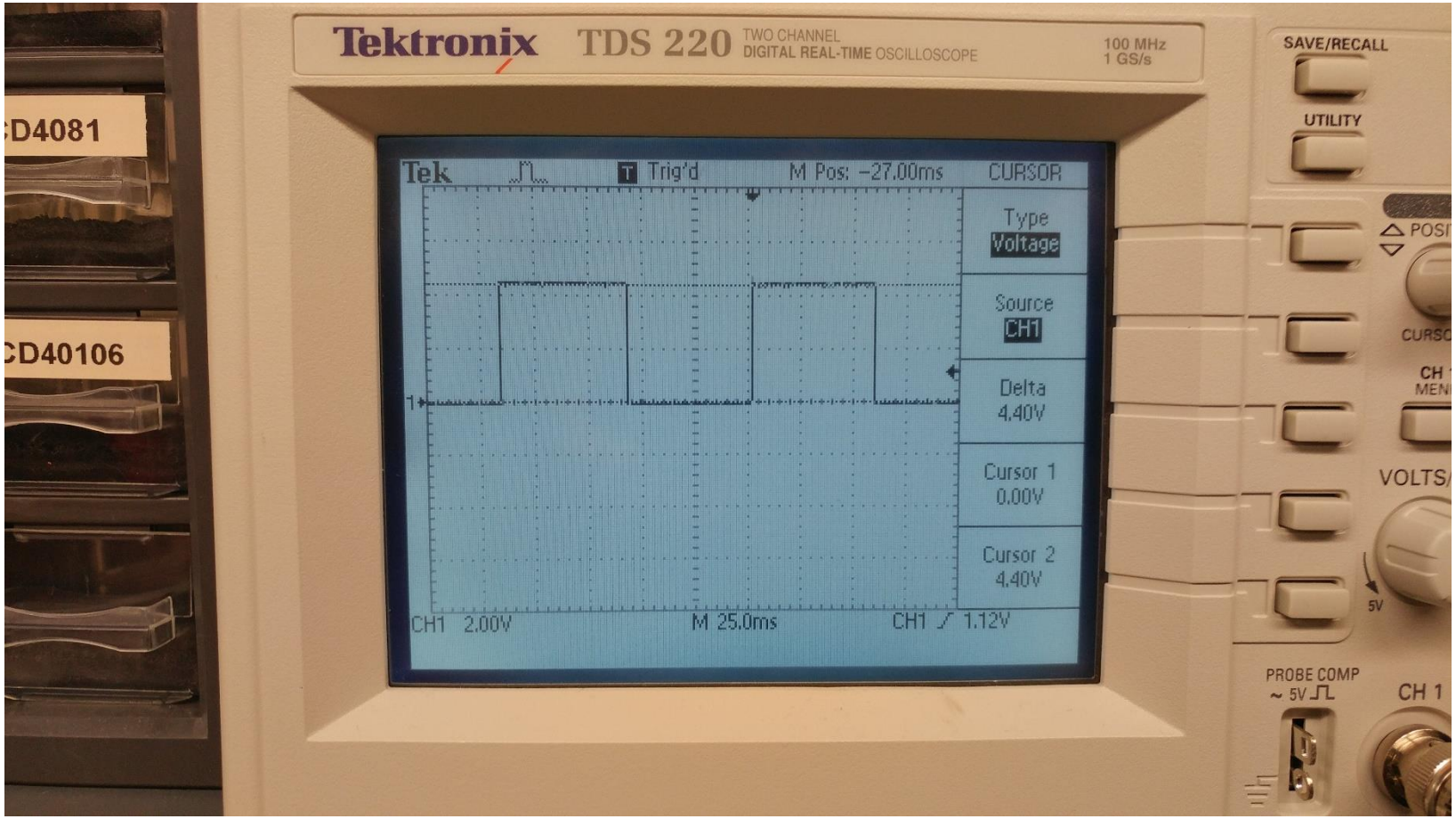

Tek
Trig'd
M Pos: -27.00ms
CH2
Coupling
DC
BW Limit
OFF
100MHz
Volts/Div
Coarse
Probe
1X
Invert
Off
CH1 2.00V
M 25.0ms
CH1 1.12V
UTILITY
PROBE COMP
~ 5V

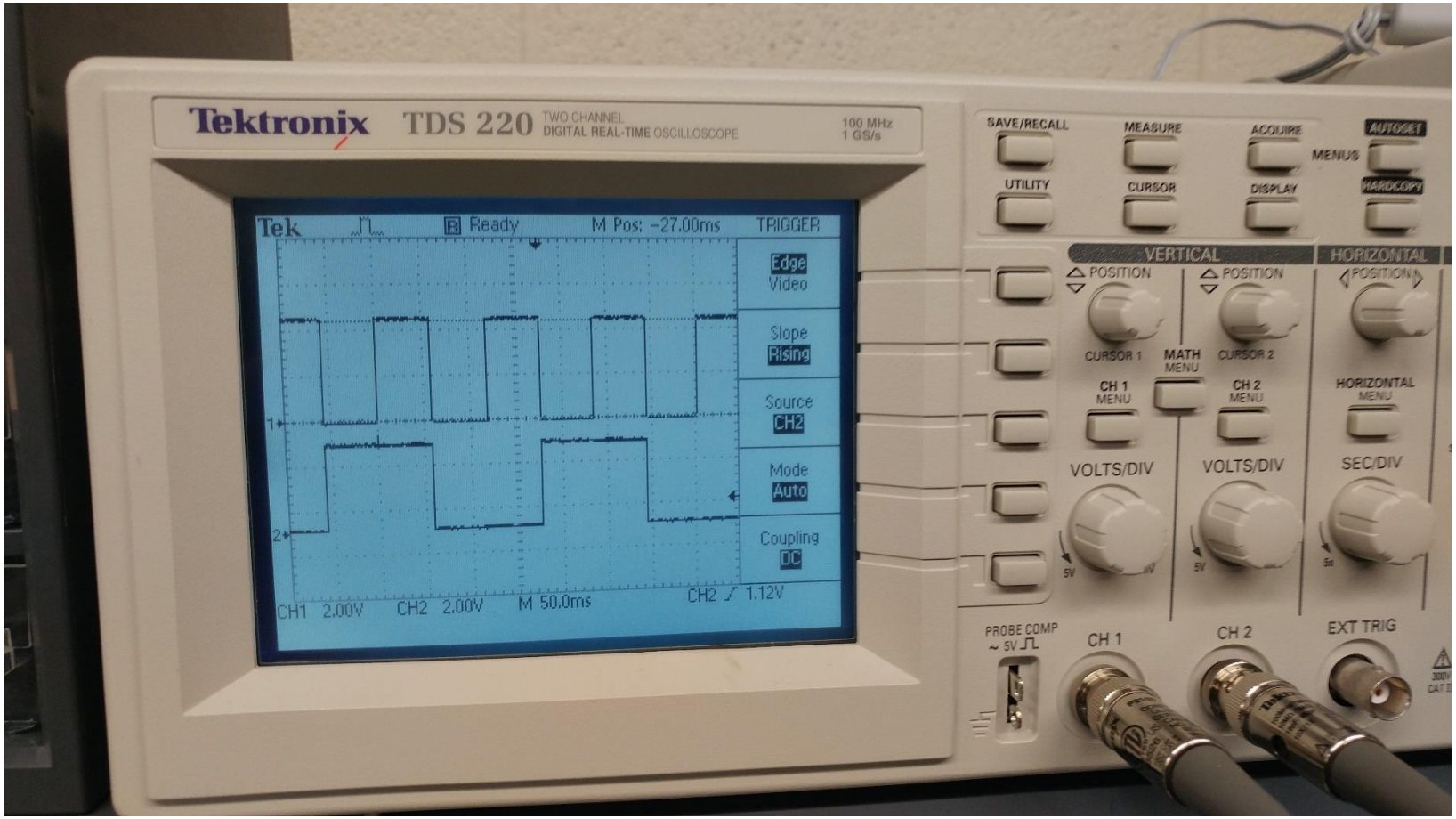

Tektronix
TDS 220
TWO CHANNEL
DIGITAL REAL-TIME OSCILLOSCOPE
100 MHz
1 GS/s
SAVE/RECALL
UTILITY
Tek
Trig'd
M Pos: -27.00ms
MEASURE
Source
Type
CH1
Freq
8.511Hz
CH1
Freq
8.511Hz
CH2 Off
Freq
CH2 Off
Pk-Pk
CH1 2.00V
M 25.0ms
CH1 1.12V
PROBE COMP
~ 5V
081
40106

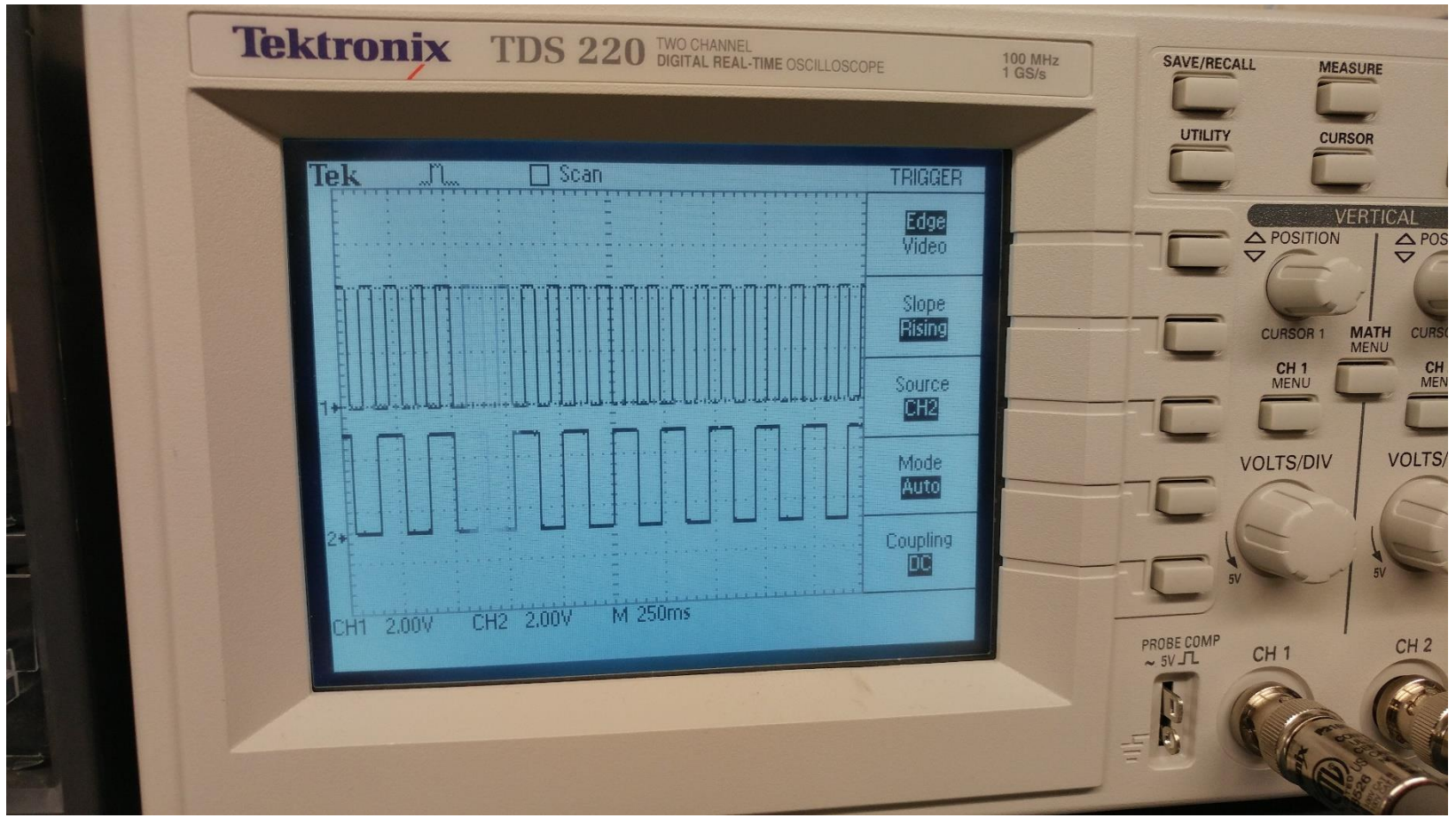

PRECISION
9425
SP9024
DM74LS73AN
1 2 3 4

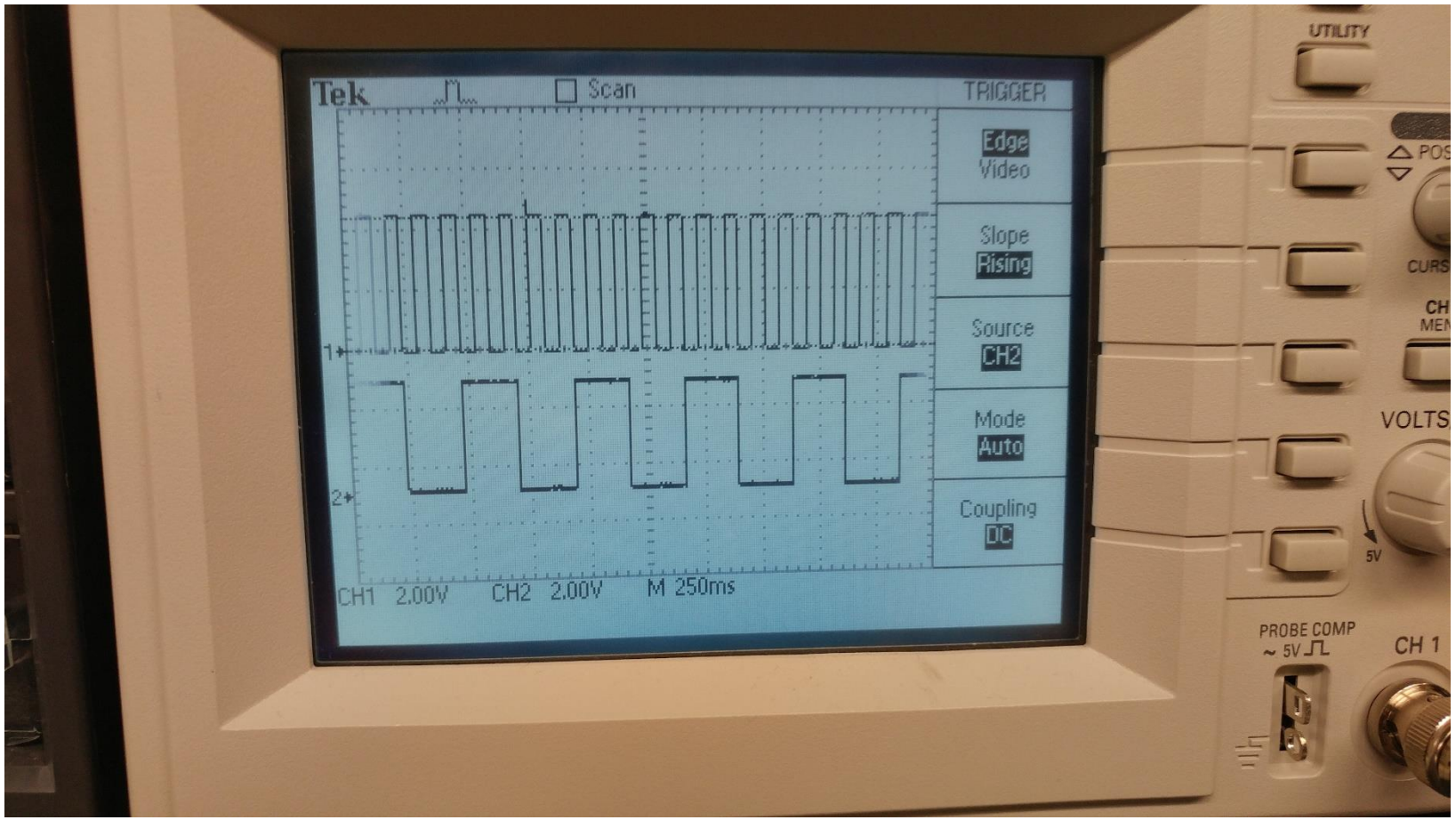

Tek
Ready
M Pos: -27.00ms
CURSOR
Type
Time
Source
CH1
Delta
59.00ms
16.95Hz
Cursor 1
-59.00ms
Cursor 2
0.000s
CH1 2.00V
M 25.0ms
CH1 ∕ 1.12V
PROBE COM
~ 5V

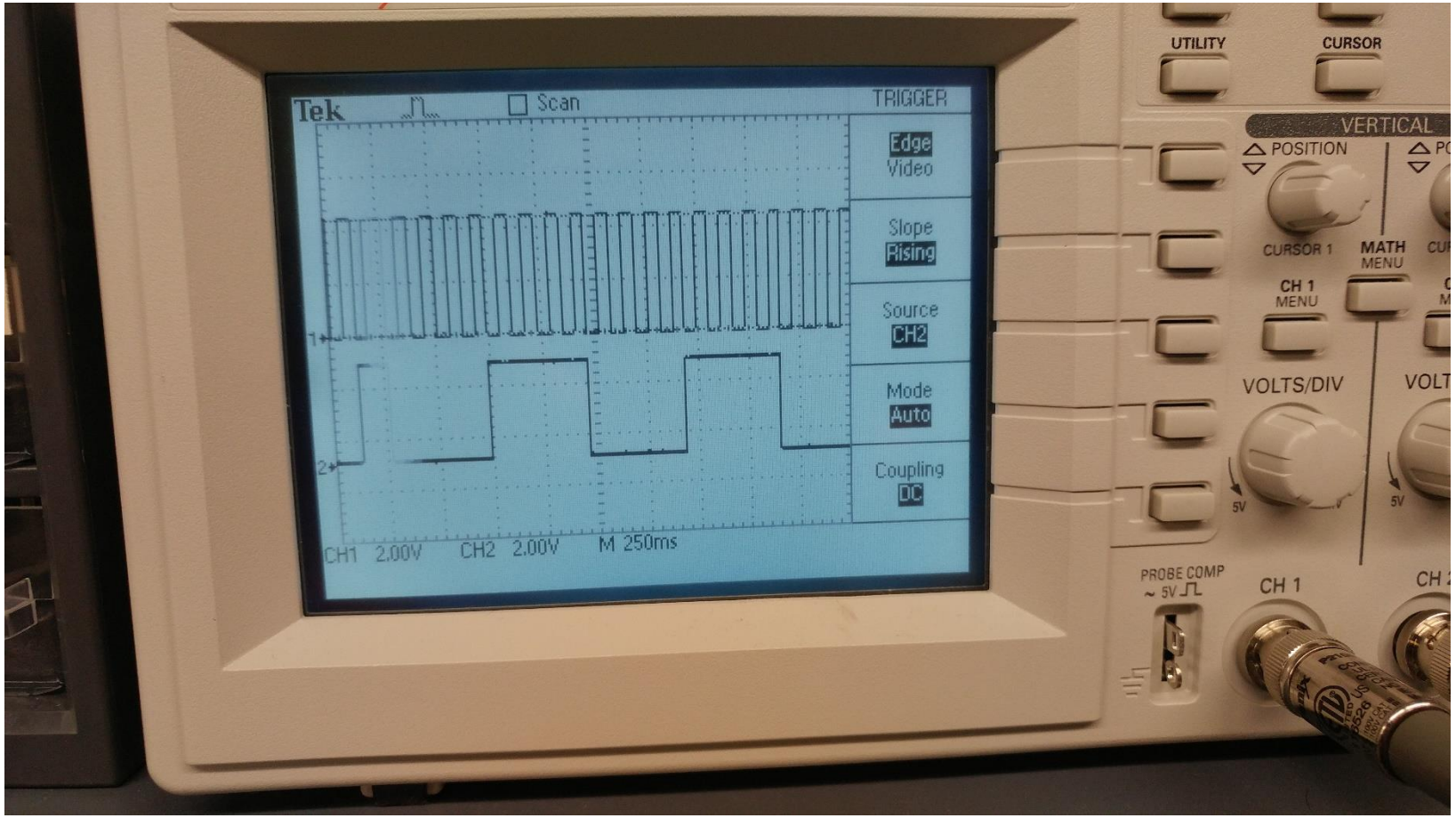

Tek
Trig'd
M Pos: -27.00ms
CURSOR
Type
Time
Source
CH1
Delta
59.00ms
16.95Hz
Cursor 1
-118.0ms
Cursor 2
-59.00ms
CH1 2.00V
M 25.0ms
CH1 1.12V
PROBE
~ 5V

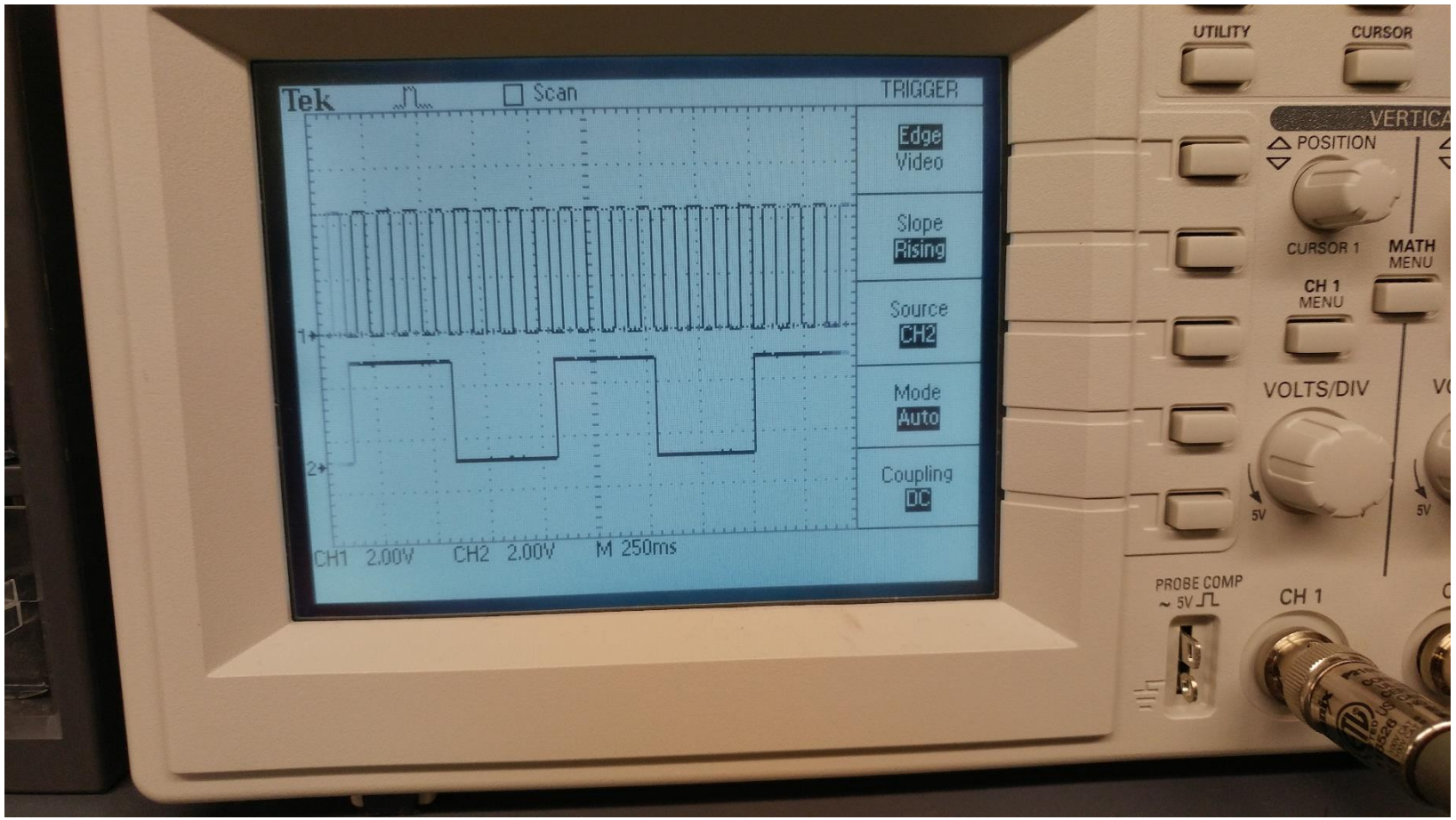

CD4081
CD40106
Tektronix
TDS 220
TWO CHANNEL
DIGITAL REAL-TIME OSCILLOSCOPE
100 MHz
1 GS/s
SAVE/RECALL
UTILITY
Tek
Trig'd
M Pos: -27.00ms
CURSOR
Type
Voltage
Source
CH1
Delta
4.40V
Cursor 1
0.00V
Cursor 2
4.40V
CH1 2.00V
M 25.0ms
CH1 1.12V
VOLTS/
5V
PROBE COMP
~ 5V
CH 1

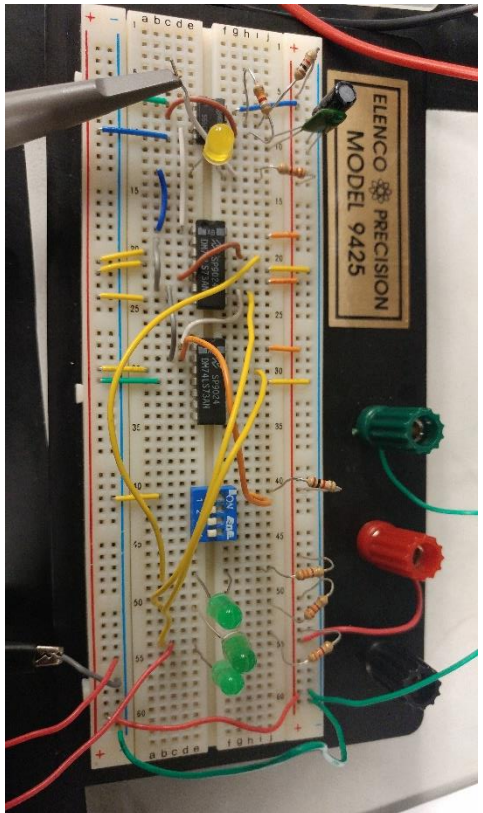

Tektronix
TDS 220
TWO CHANNEL
DIGITAL REAL-TIME OSCILLOSCOPE
100 MHz
1 GS/s
Tek
Ready
M Pos: -27.00ms
TRIGGER
Edge
Video
Slope
Rising
Source
CH2
Mode
Auto
Coupling
DC
CH1 2.00V
CH2 2.00V
M 50.0ms
CH2 1.12V
SAVE/RECALL
MEASURE
ACQUIRE
MENUS
AUTOSET
UTILITY
CURSOR
DISPLAY
HARDCOPY
VERTICAL
HORIZONTAL
POSITION
CURSOR 1
MATH
MENU
CURSOR 2
CH 1
MENU
CH 2
MENU
HORIZONTAL
MENU
VOLTS/DIV
VOLTS/DIV
SEC/DIV
PROBE COMP
~ 5V
CH 1
CH 2
EXT TRIG

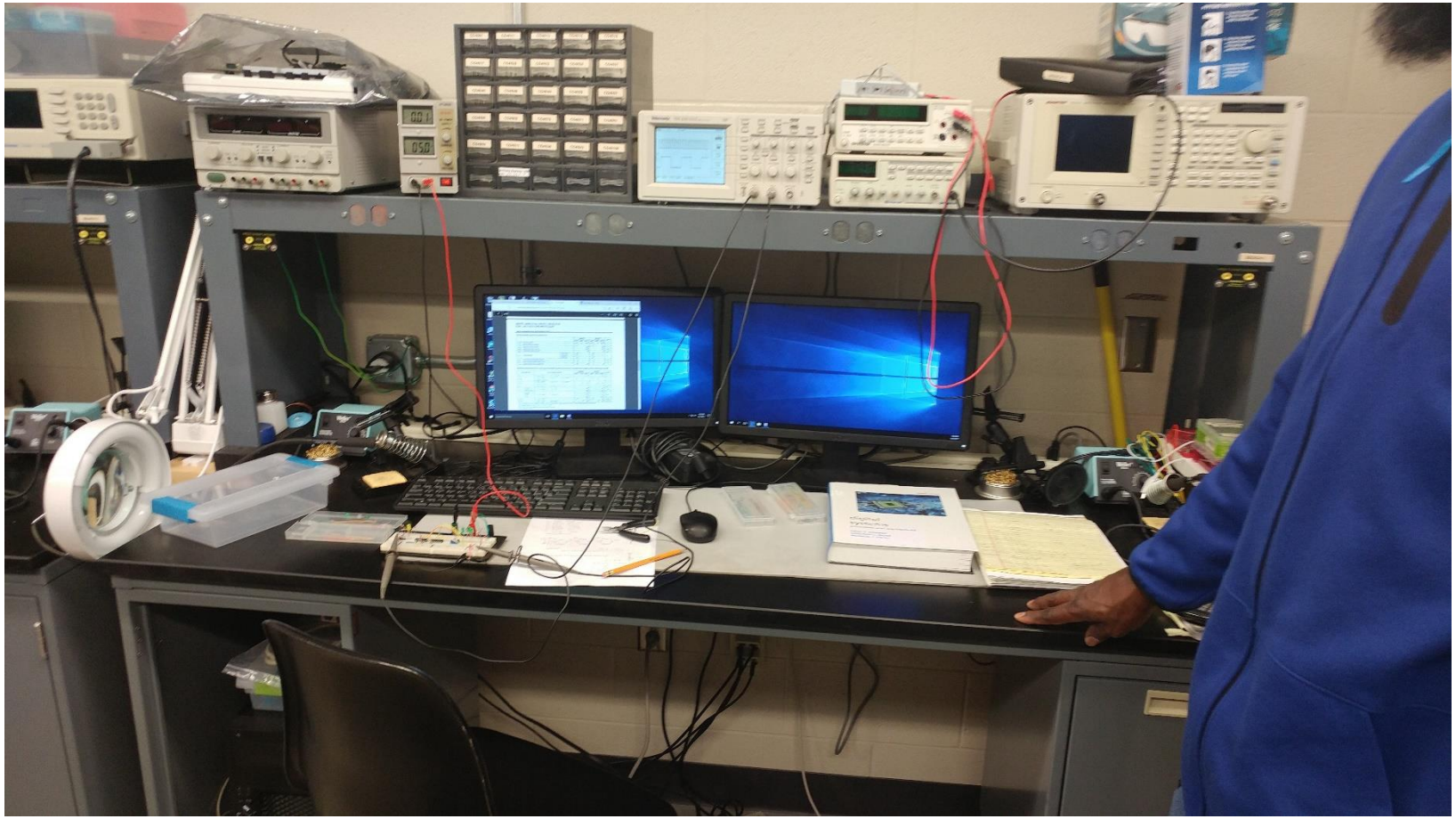

Tektronix
TDS 220
TWO CHANNEL
DIGITAL REAL-TIME OSCILLOSCOPE
100 MHz
1 GS/s
SAVE/RECALL
MEASURE
UTILITY
CURSOR
VERTICAL
POSITION
CURSOR 1
MATH
MENU
CH 1
MENU
VOLTS/DIV
5V
PROBE COMP
~ 5V
CH 1
CH 2
Tek
Scan
TRIGGER
Edge
Video
Slope
Rising
Source
CH2
Mode
Auto
Coupling
DC
CH1 2.00V
CH2 2.00V
M 250ms


Tek
Scan
TRIGGER
Edge
Video
Slope
Rising
Source
CH2
Mode
Auto
Coupling
DC
CH1 2.00V
CH2 2.00V
M 250ms
UTILITY
VOLTS
5V
PROBE COMP
~ 5V
CH 1

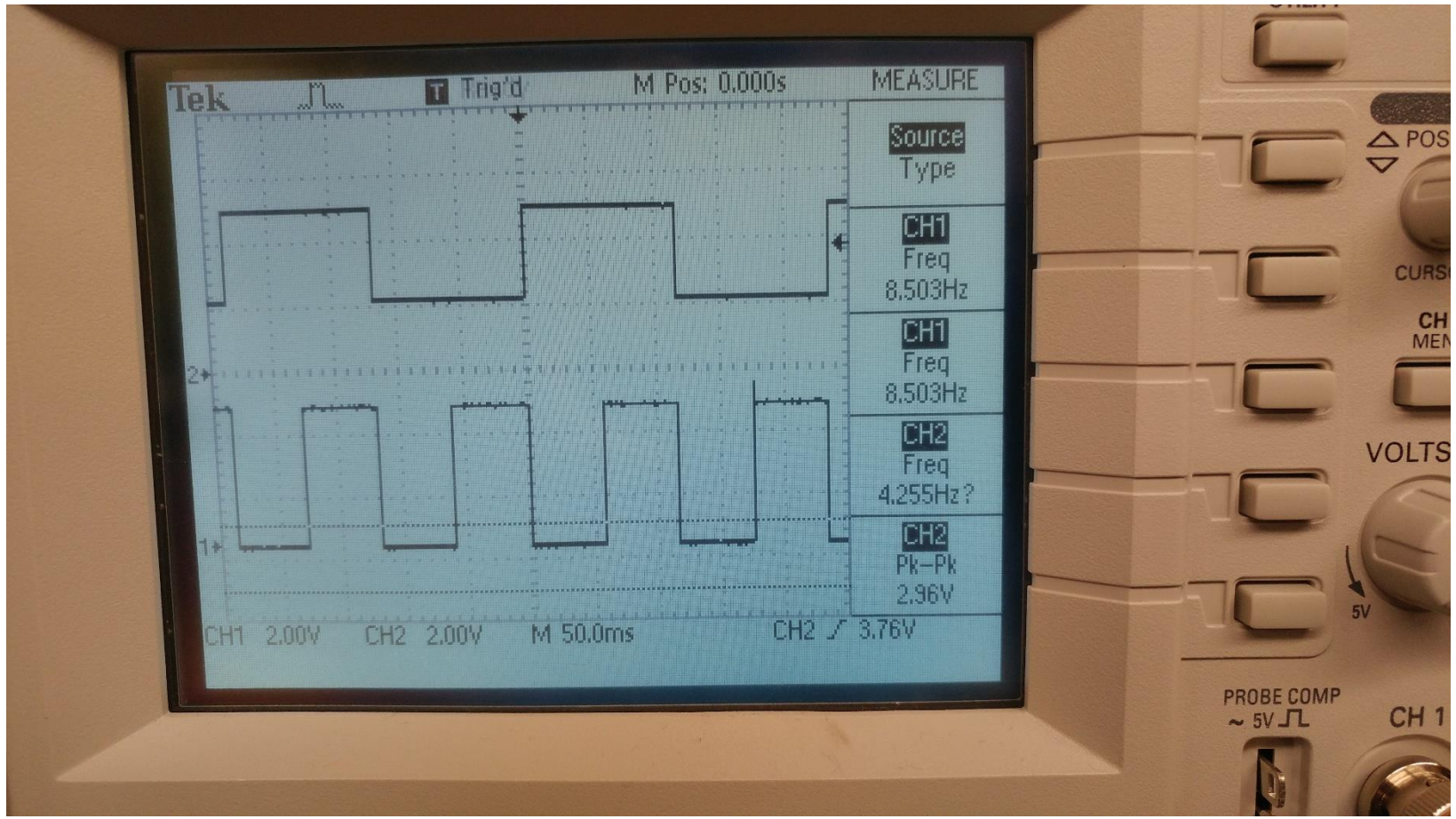

Tek
Scan
TRIGGER
Edge
Video
Slope
Rising
Source
CH2
Mode
Auto
Coupling
DC
CH1 2.00V
CH2 2.00V
M 250ms
UTILITY
CURSOR
VERTICAL
POSITION
CURSOR 1
MATH
MENU
CH 1
MENU
VOLTS/DIV
5V
PROBE COMP
~ 5V
CH 1

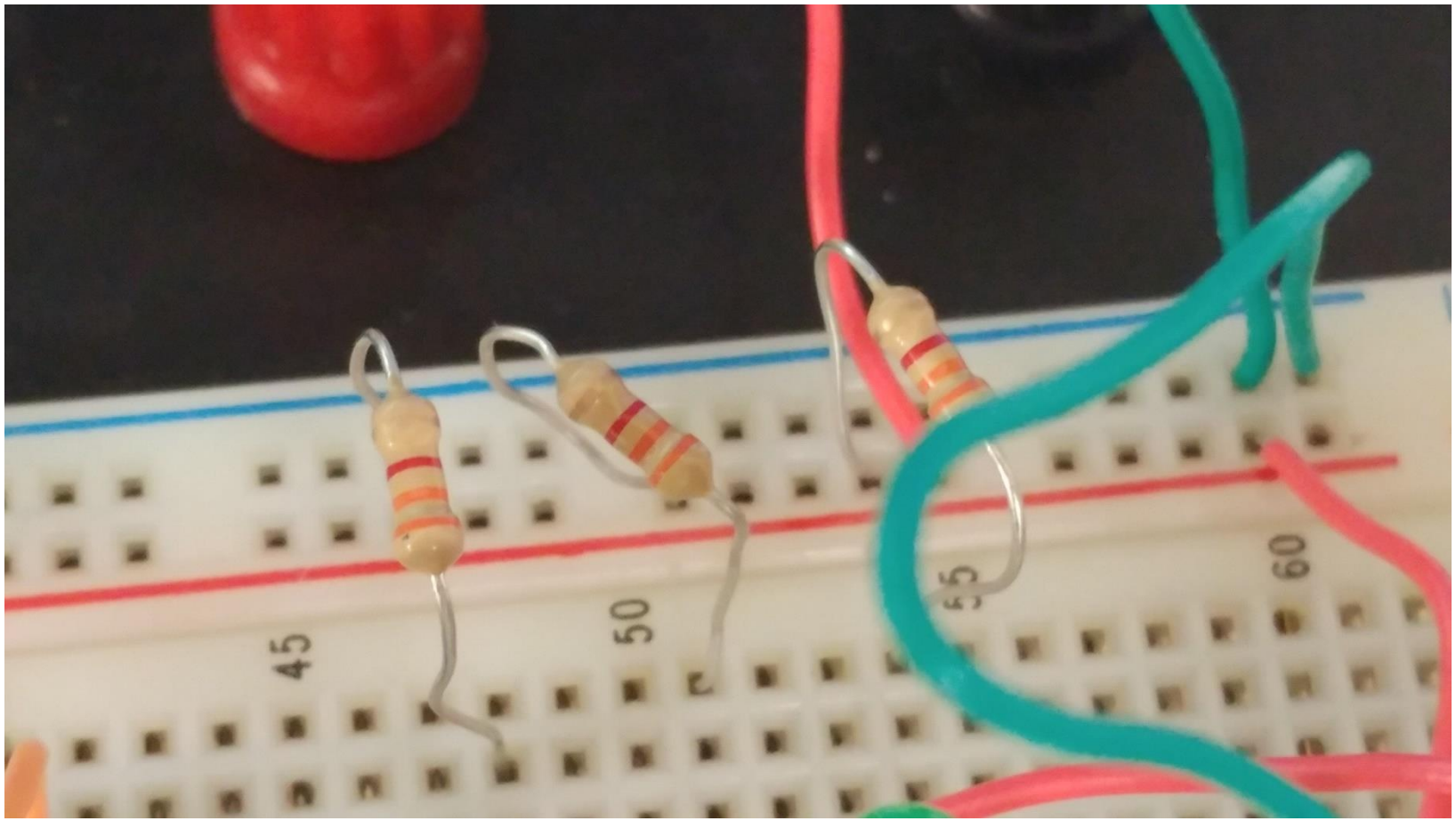

Tek
Scan
TRIGGER
Edge
Video
Slope
Rising
Source
CH2
Mode
Auto
Coupling
DC
CH1 2.00V
CH2 2.00V
M 250ms
UTILITY
CURSOR
POSITION
CURSOR 1
MATH
MENU
CH 1
MENU
VOLTS/DIV
5V
PROBE COMP
~ 5V
CH 1

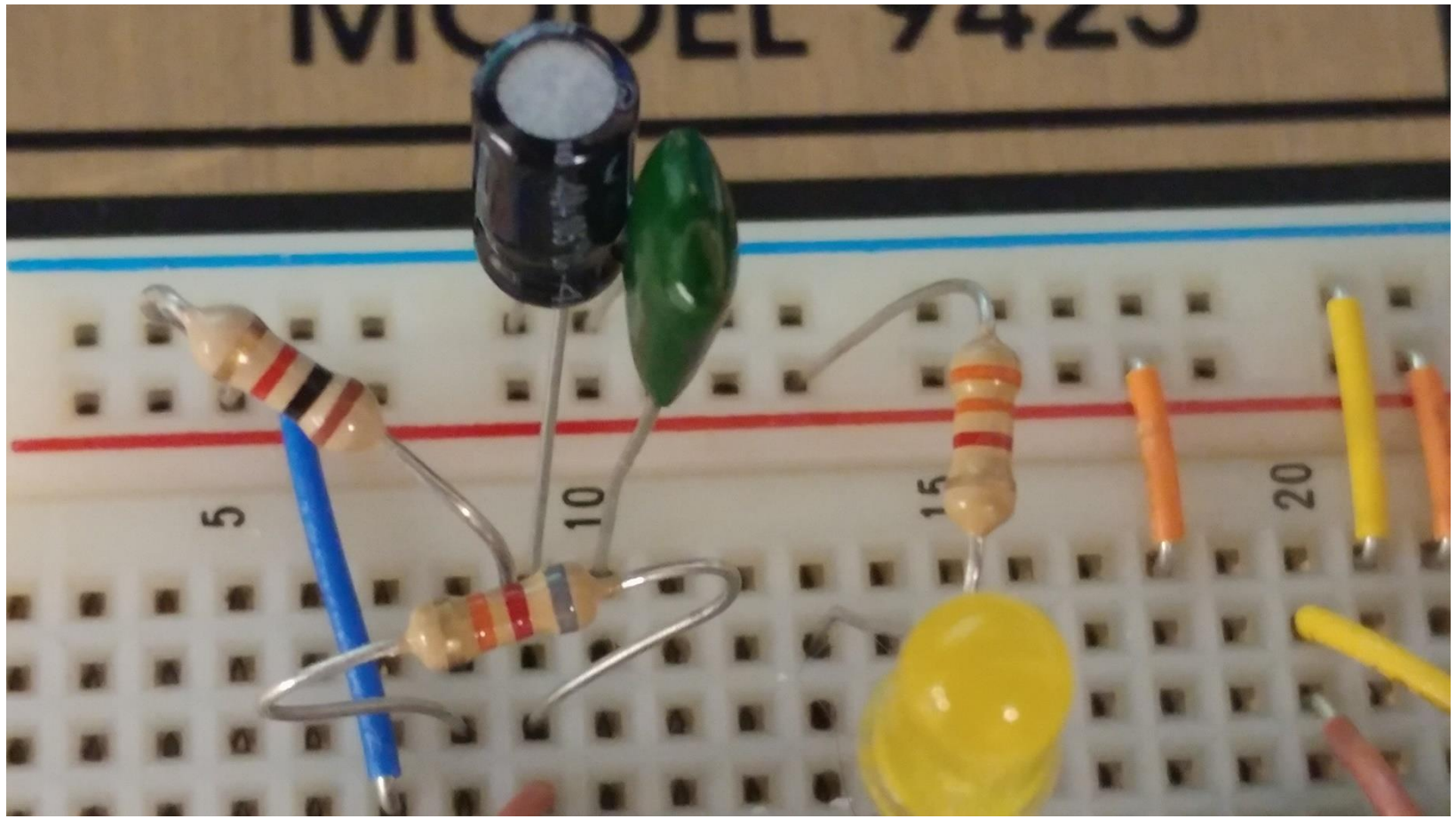

ELENCO
PRECISION
MODEL 9425

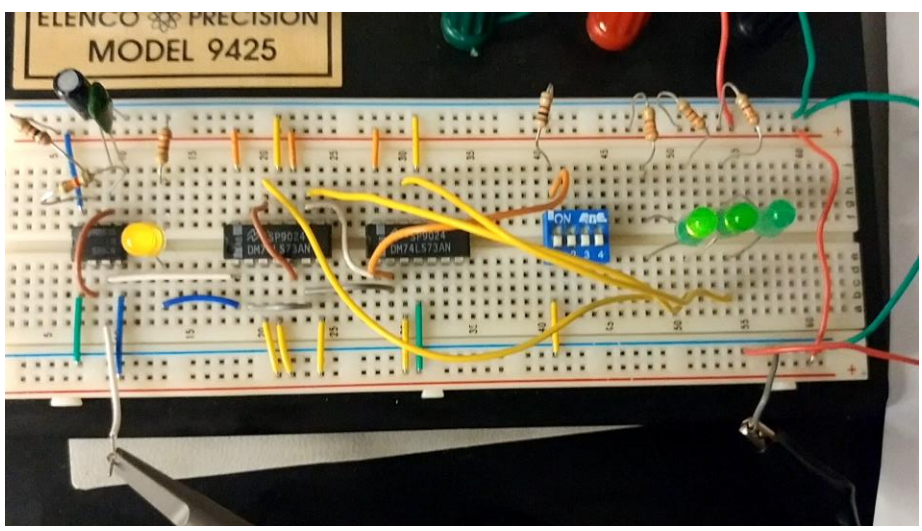


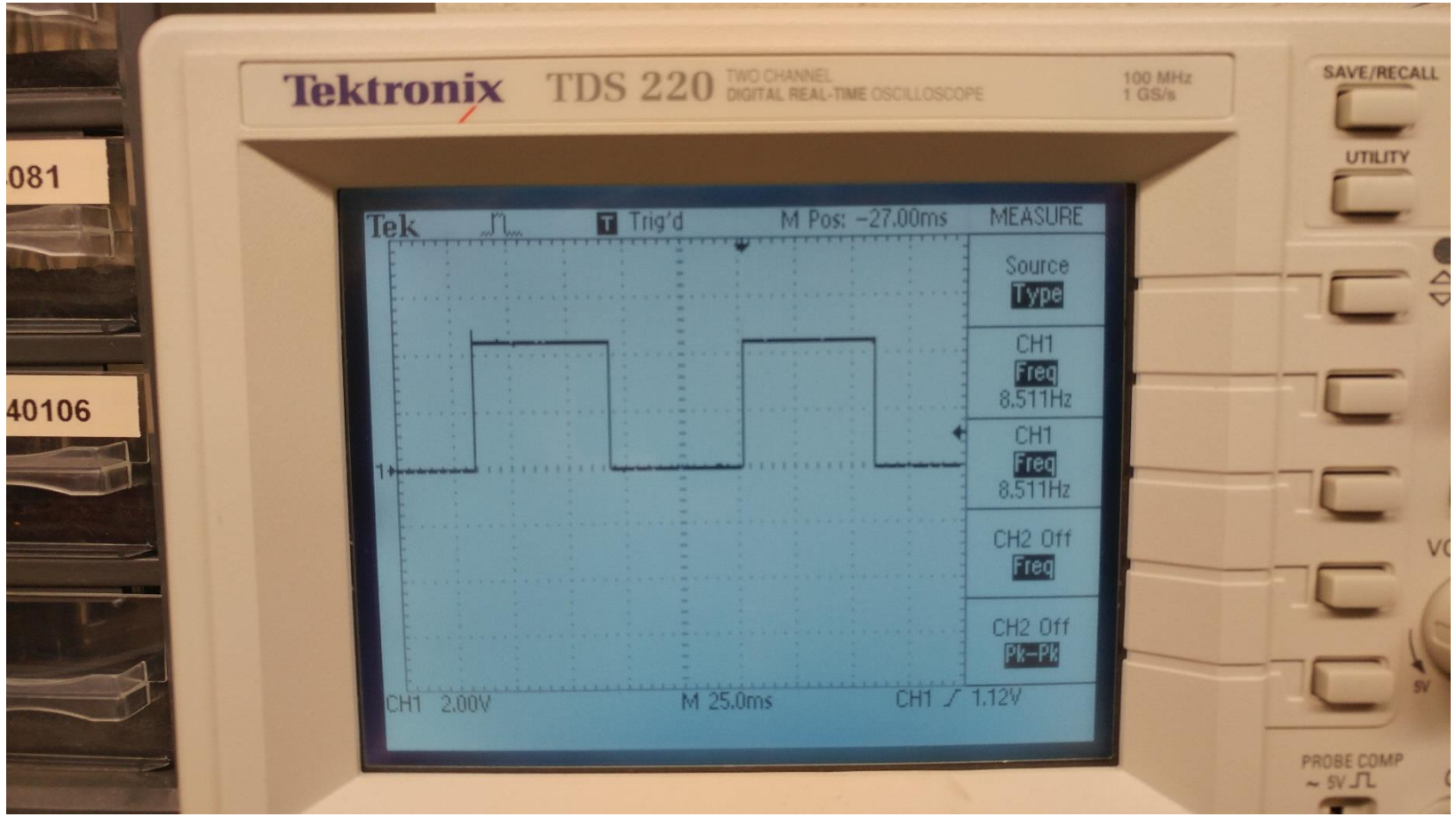

BENCH 1
WRIST STRAP GROUND
09740
DESCO
www.desco.com
MADE IN AMERICA

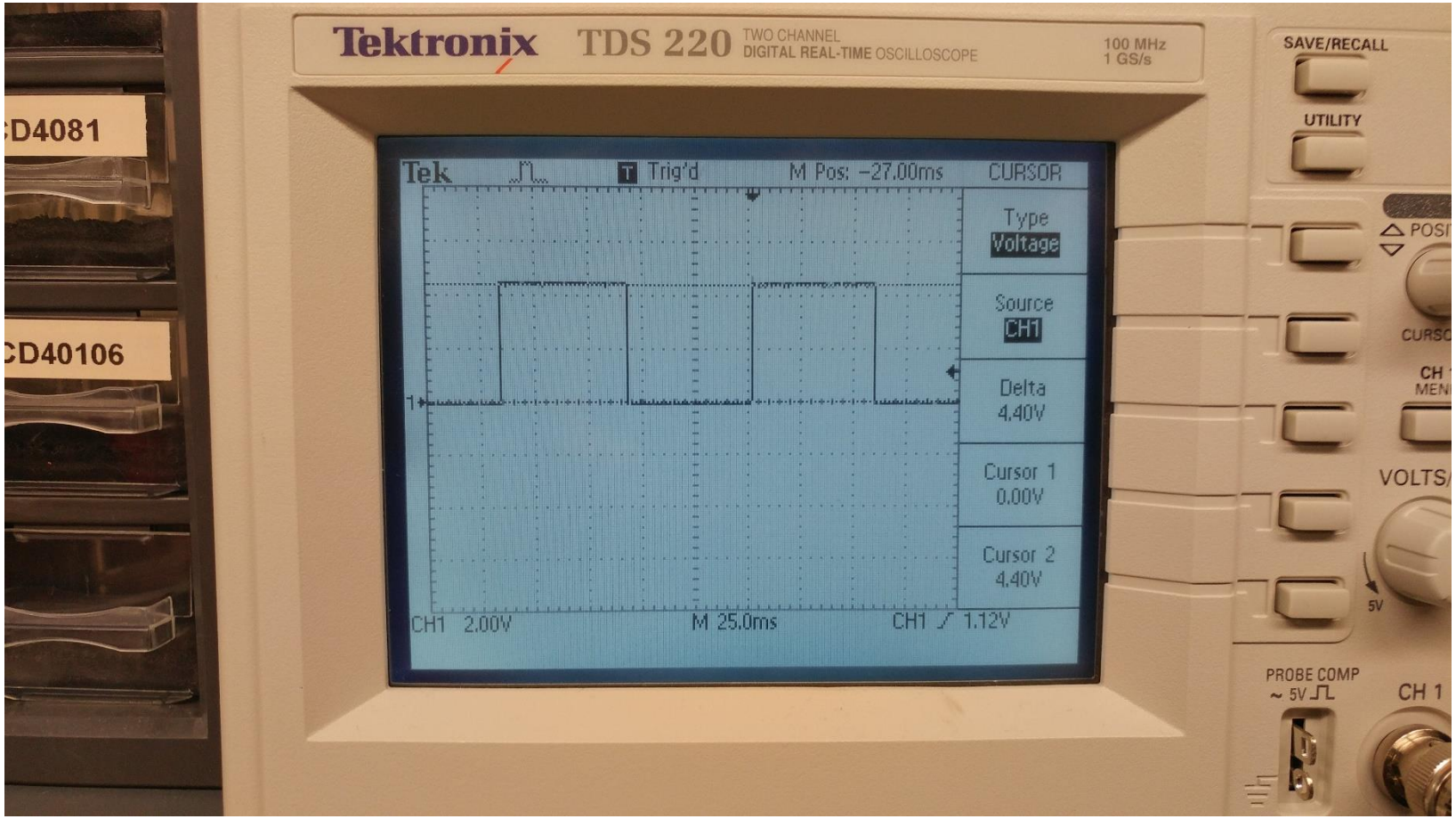

Tek
Trig'd
M Pos: 0.000s
MEASURE
Source
Type
CH1
Freq
8.503Hz
CH1
Freq
8.503Hz
CH2
Freq
4.255Hz?
CH2
Pk-Pk
2.96V
CH1 2.00V
CH2 2.00V
M 50.0ms
CH2 3.76V
POS
VOLTS
5V
PROBE COMP
~ 5V
CH 1

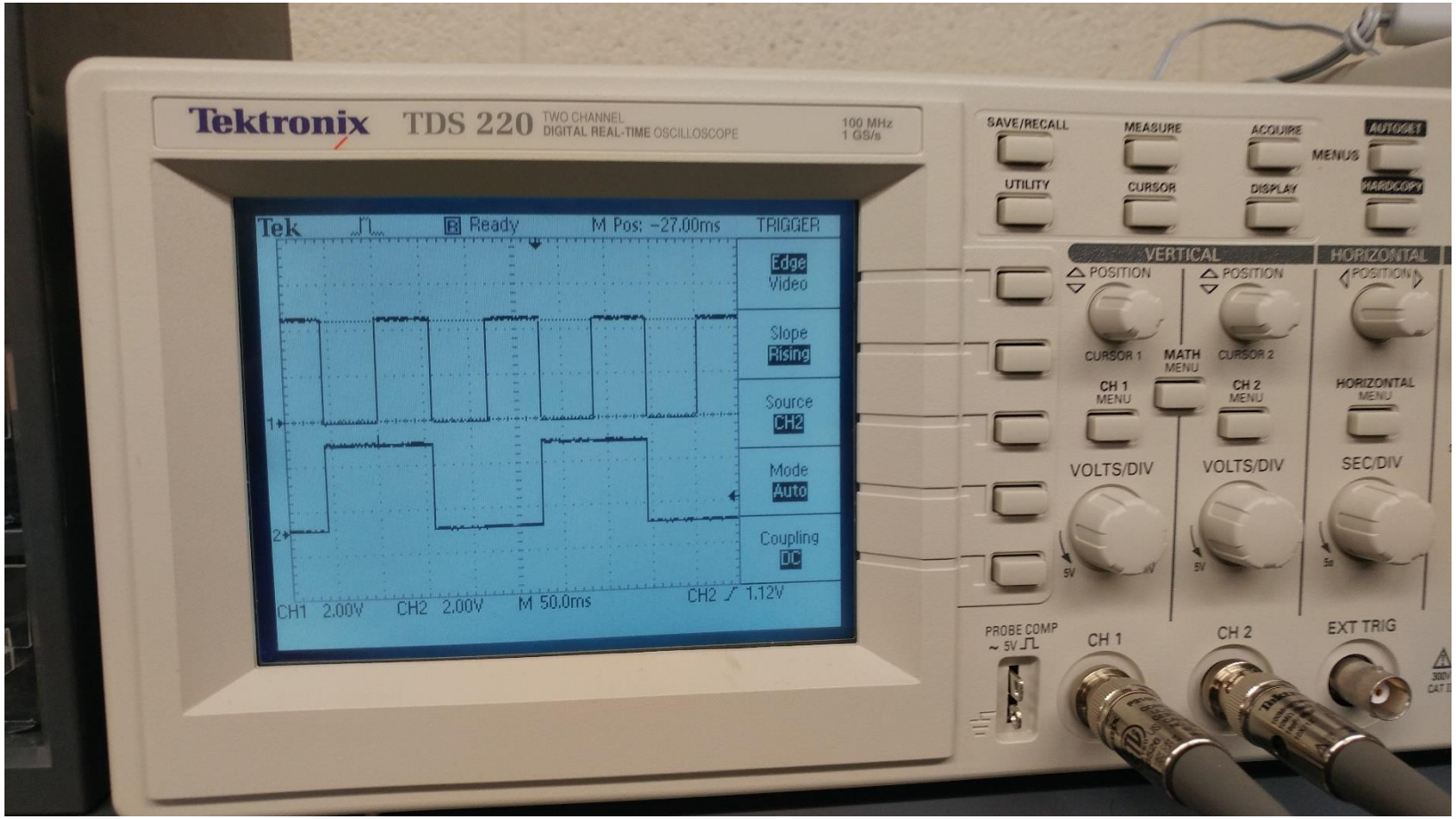

45
50
55
60

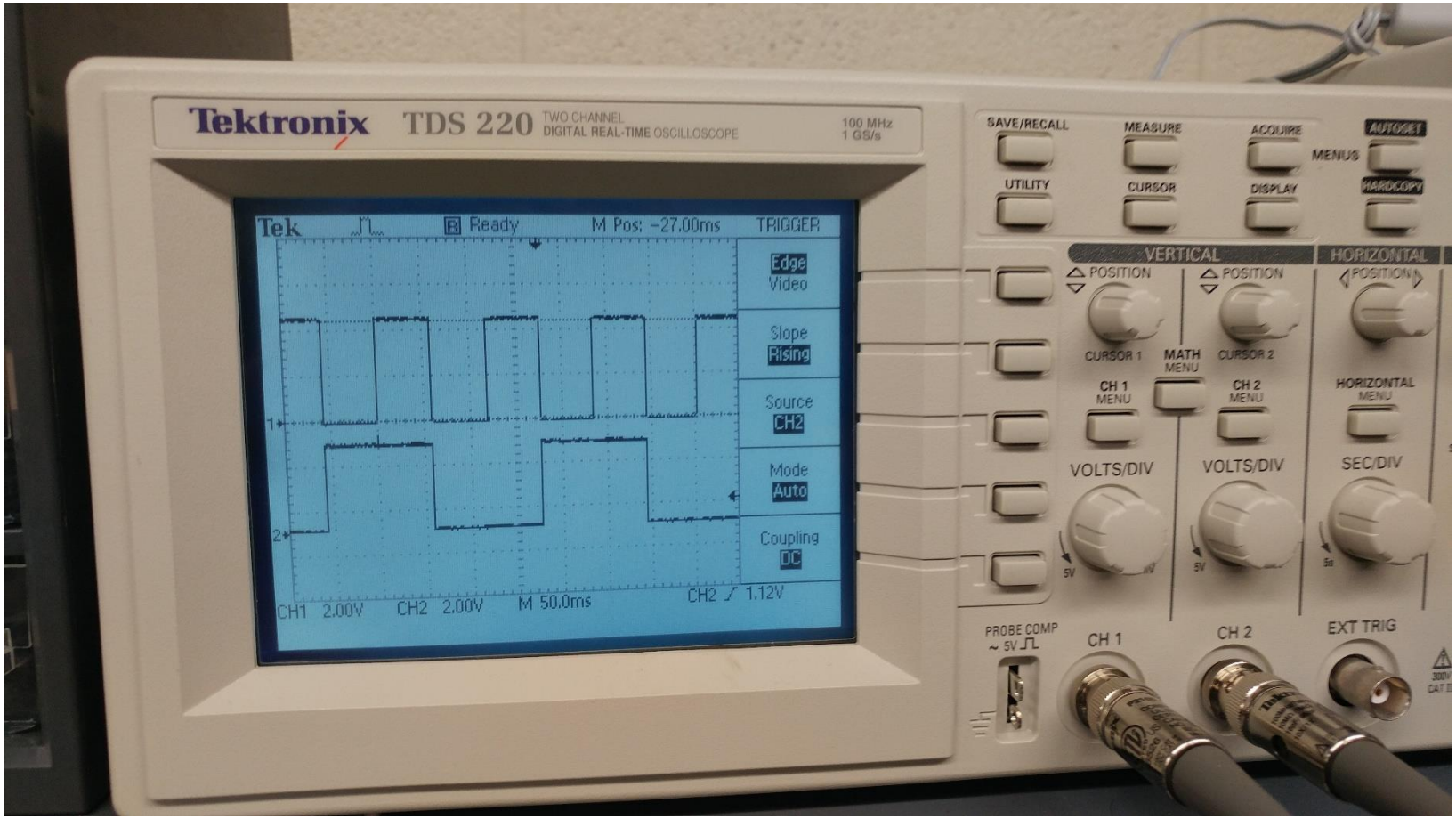

5
10
15
20

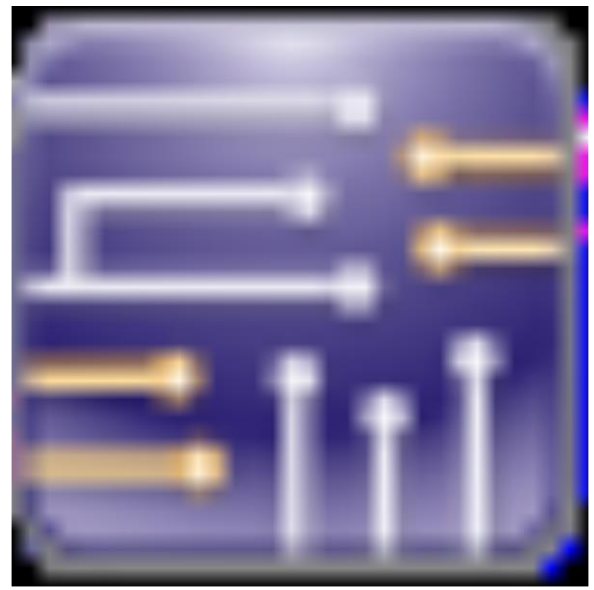

ELENCO PRECISION
MODEL 9425
ON
DM74LS73AN


Tektronix
TDS 220
TWO CHANNEL
DIGITAL REAL-TIME OSCILLOSCOPE
100 MHz
1 GS/s
SAVE/RECALL
UTILITY
Tek
Trig'd
M Pos: -27.00ms
MEASURE
Source
Type
CH1
Freq
8.511Hz
CH1
Freq
8.511Hz
CH2 Off
Freq
CH2 Off
Pk-Pk
CH1 2.00V
M 25.0ms
CH1 1.12V
PROBE COMP
~ 5V
081
40106


CD4081
CD40106
Tektronix
TDS 220
TWO CHANNEL
DIGITAL REAL-TIME OSCILLOSCOPE
100 MHz
1 GS/s
SAVE/RECALL
UTILITY
Tek
Trig'd
M Pos: -27.00ms
CURSOR
Type
Voltage
Source
CH1
Delta
4.40V
Cursor 1
0.00V
Cursor 2
4.40V
CH1 2.00V
M 25.0ms
CH1 1.12V
VOLTS/
5V
PROBE COMP
~ 5V
CH 1


Tektronix
TDS 220
TWO CHANNEL
DIGITAL REAL-TIME OSCILLOSCOPE
100 MHz
1 GS/s
Tek
Ready
M Pos: -27.00ms
TRIGGER
Edge
Video
Slope
Rising
Source
CH2
Mode
Auto
Coupling
DC
CH1 2.00V
CH2 2.00V
M 50.0ms
CH2 1.12V
SAVE/RECALL
MEASURE
ACQUIRE
MENUS
AUTOSET
UTILITY
CURSOR
DISPLAY
HARDCOPY
VERTICAL
HORIZONTAL
POSITION
CURSOR 1
MATH
MENU
CURSOR 2
CH 1
MENU
CH 2
MENU
HORIZONTAL
MENU
VOLTS/DIV
VOLTS/DIV
SEC/DIV
PROBE COMP
~ 5V
CH 1
CH 2
EXT TRIG

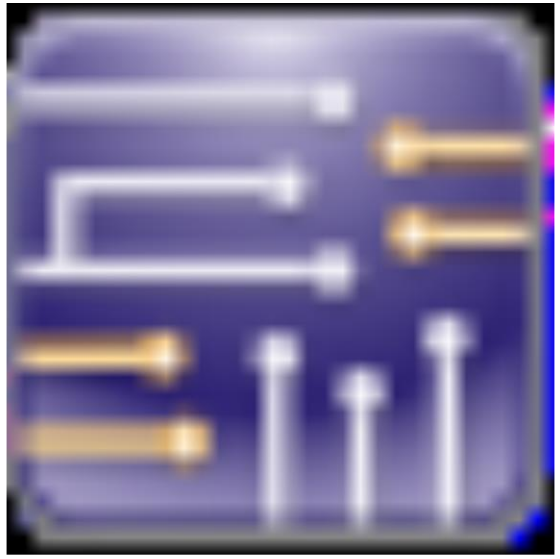

Tektronix
TDS 220
TWO CHANNEL
DIGITAL REAL-TIME OSCILLOSCOPE
100 MHz
1 GS/s
Tek
Ready
M Pos: -27.00ms
TRIGGER
Edge
Video
Slope
Rising
Source
CH2
Mode
Auto
Coupling
DC
CH1 2.00V
CH2 2.00V
M 50.0ms
CH2 1.12V
SAVE/RECALL
MEASURE
ACQUIRE
MENUS
AUTOSET
UTILITY
CURSOR
DISPLAY
HARDCOPY
VERTICAL
HORIZONTAL
POSITION
CURSOR 1
MATH
MENU
CURSOR 2
CH 1
MENU
CH 2
MENU
HORIZONTAL
MENU
VOLTS/DIV
VOLTS/DIV
SEC/DIV
PROBE COMP
~ 5V
CH 1
CH 2
EXT TRIG



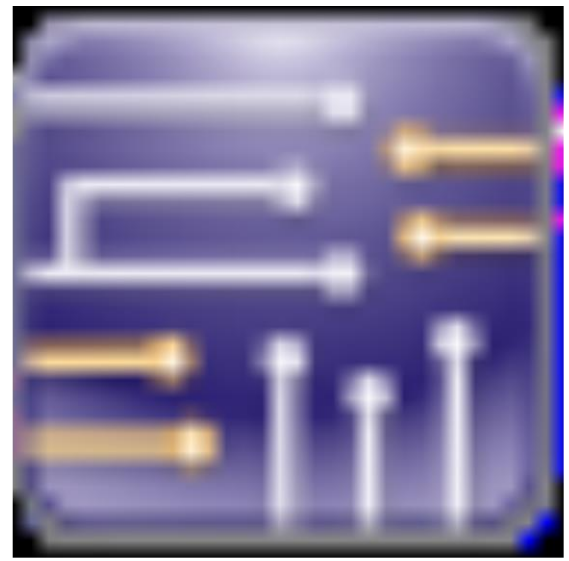
Lab(9).ms14

Lab(9)-1.ms14

Lab9-Bit counter



Lab(9)-1.ms14



555.ms14

Counter with flip-flops