EECT112 – 50C

Lab 1 – Logic Levels

Names: ___Jose Alberto Tapia_____, ____ Juddo Abaker _____
Date: ____9/8/17_____

The purpose of this lab is to:
Learn how to create logic levels for digital circuits using switches and resistors.

Select four 10kohm resistors.
Measure and record the resistance of each resistor.

Equipment needed:

1 – Digital Multimeter
4 – 10Kohm
1 – 4 position dip switch

Using Multisim simulate Figure 1 for each voltage level and record in Table 1. Then build and test and measure each voltage level and record in Table 1

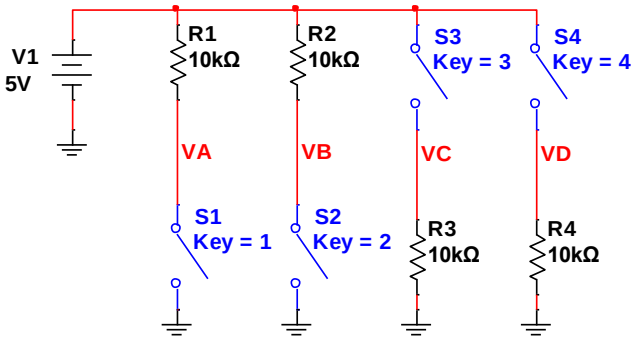

Figure 1- Lab 1 Schematic

	Simulated		Test	
	Open	Closed	Open	Closed
VA	5 V	0 V	5.03 V	0 V
VB	5 V	0 V	5.03 V	0 V
VC	0 V	5 V	0 V	5.03 V
VD	0 V	5 V	0 V	4.97 V

Table 1 (Simulation vs Test)

Observations:___Resistors: 10.016 K, 9.874 K, 9.701 K, 9.875 K.

_____

_____We observed how in a simulated environment, the values tend to neglect any other variables that could affect the outcome. Meanwhile, in the lab we noticed how values tend to change with what the professor says is the result of variable such as friction or heat that tends to change the measured voltage coming from the resistors.

_____

_____

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Lab 3 – Logic Gates

Names: STEVE KEPLER, ARAKER

Date: 9-29-17

The purpose of this lab is to:
Learn how to test AND and OR logic gates.

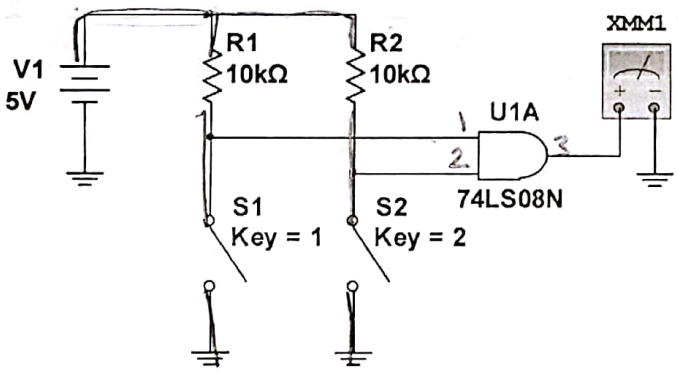
Select two 10kohm resistors.
Measure and record the resistance of each resistor.

Equipment needed:

1 – Digital Multimeter
2 – 10Kohm
1 – 4 position dip switch
1 – 74LS08
1 – 74LS32

S1	S2	SIM	LAB
CLOSE	CLOSE	0 V	0.16 V
CLOSE	OPEN	0 V	0-16V
OPEN	CLOSE	0V	0-16V
OPEN	OPEN	5 V	4-38V

Using Multisim simulate Figure 1 for each voltage level and record in Table 1. Then build, test and measure each voltage level and record in Table 1



	Simulated		Test	
	Open	Closed	Open	Closed
S1				
S2				

Table 1 (Simulation vs Test)

Figure 1- Lab 3 Schematic

Using Multisim simulate Figure 2 for each voltage level and record in Table 2. Then build, test and measure each voltage level and record in Table 2

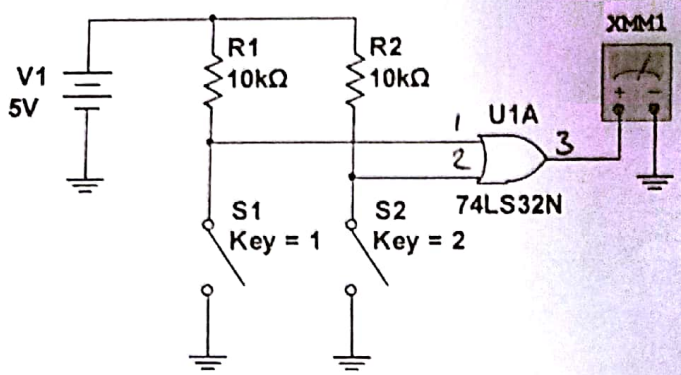


Figure 2 - Lab 3 Schematic

	Simulated		Test	
	Open	Closed	Open	Closed
S1				
S2				

Table 2 (Simulation vs Test)

S1	S2	SIM	LAB
CLOSE	CLOSE	0V	0.12V
CLOSE	OPEN	5V	4.06V
OPEN	CLOSE	5V	4.06V
OPEN	OPEN	5V	4.06V

SWITCH CLOSED = LOGIC 0

SWITCH OPEN = LOGIC 1

Observations:

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Lab 4 – Lecture 3b Slide 3

Names: Judd Abaka Steve Kepcer
Date: 10/6/17

The purpose of this lab is to:
Learn more about describing Logic Circuits algebraically.

$V = IR$
$0 = (0)(10k)$
$I = \frac{V}{R} = \frac{5}{10,000}$
$= .5\,mA$

Select three 10kohm resistors.
Measure and record the resistance of each resistor.

Equipment needed:

1 – Digital Multimeter
3 – 10Kohm
1 – 4 position dip switch
1 – 74LS08
1 – 74LS32

Using Multisim simulate Figure 1 for each voltage level and record in Table 1. Then build, test and measure each voltage level and record in Table 1

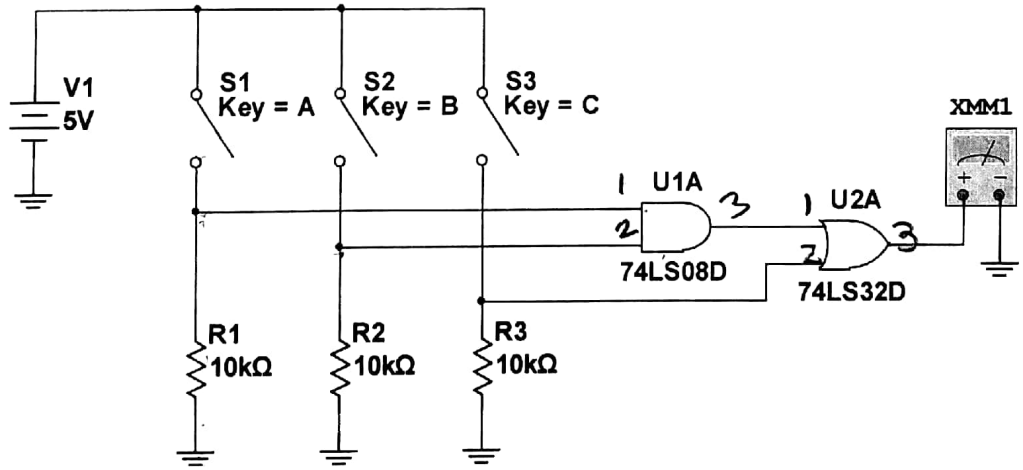

Figure 1- Lab 4 Schematic

	Simulated		Test	
	Open	Closed	Open	Closed
S1				
S2				
S3				

Table 1 (Simulation vs Test)

S1	S2	S3	OUT SIM	OUT LAB
0	0	0		0
0	0	0		1
0	1	0		0
0	1	1		1
1	0	0		0
1	0	1		1
1	1	0		1
1	1	1		1

Using Multisim simulate Figure 2 for each voltage level and record in Table 2. Then build, test and measure each voltage level and record in Table 2

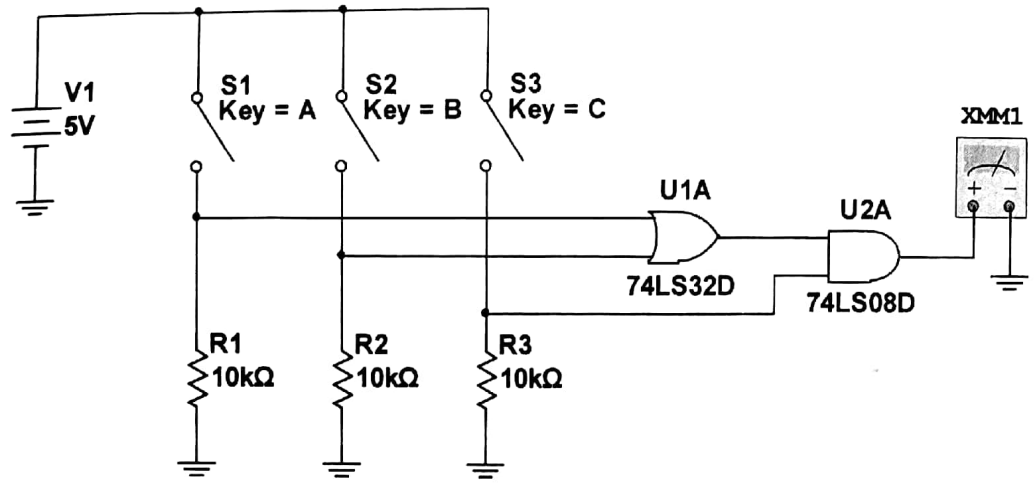

Figure 2 - Lab 4 Schematic

	Simulated		Test	
	Open	Closed	Open	Closed
S1				
S2				
S3				

Table 2 (Simulation vs Test)

S1	S2	S3	OUT SIM	OUT LAB
0	0	0		0
0	0	1		0
0	1	0		0
0	1	1		1
1	0	0		0
1	0	1		1
1	1	0		0
1	1	1		1

Observations: 10 kΩ RESISTORS DO NOT WORK RELIABLY. 1 kΩ DOES.

LAB 4

FIGURE 1

AND / OR

S1	S2	S3	1*2	(1*2)+3
0	0	0	0	0
0	0	1	0	1
0	1	0	0	0
0	1	1	0	1
1	0	0	0	0
1	0	1	0	1
1	1	0	1	1
1	1	1	1	1

	w/ 10 kΩ	w/ 1 kΩ
FALSE	0.07	0-074
TRUE ✓	4.47	4-46
FALSE	1.41	0-07
TRUE ✓	4.46	4-46
FALSE	1.48	0-07
TRUE ✓	4.47	4-46
TRUE ✓	4.46	4-46
TRUE ✓	4.46	4-46

FIGURE 2

OR / AND

S1	S2	S3	1+2	(1+2)*3
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	1	1

FALSE	0-13
FALSE	0-13
FALSE	0-13
TRUE	4-43
FALSE	0-13
TRUE	4-43
FALSE	0-14
TRUE	4-43

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Lab 7 – Circuit Reduction (Part 1)

Names: Bret Barnett, Juddo Abaker, Steve Kepler
Date: 10-27-17

The purpose of this lab is to:
Learn how to reduce a circuit design down to the smallest size using the 17 Theorems and Karnaugh maps. Part 2 will explore how to reduce the circuit.

Select two 10kohm resistors.
Measure and record the resistance of each resistor.

Equipment needed:

1 – Digital Multimeter
3 – 10Kohm
1 – 4 position dip switch
1 – 74LS04 Hex Inverter
1 – 74LS00 Quad NAND
1 – 74LS11 Triple 3 input AND
1 – 74LS32 Quad OR

$\overline{A \cdot B} = \bar{A} + \bar{B}$

$\overline{A + B} = \bar{A} \cdot \bar{B}$

Using Multisim simulate Figure 1 for each input and record in Table 1. Then build and test circuit and record in Table 1

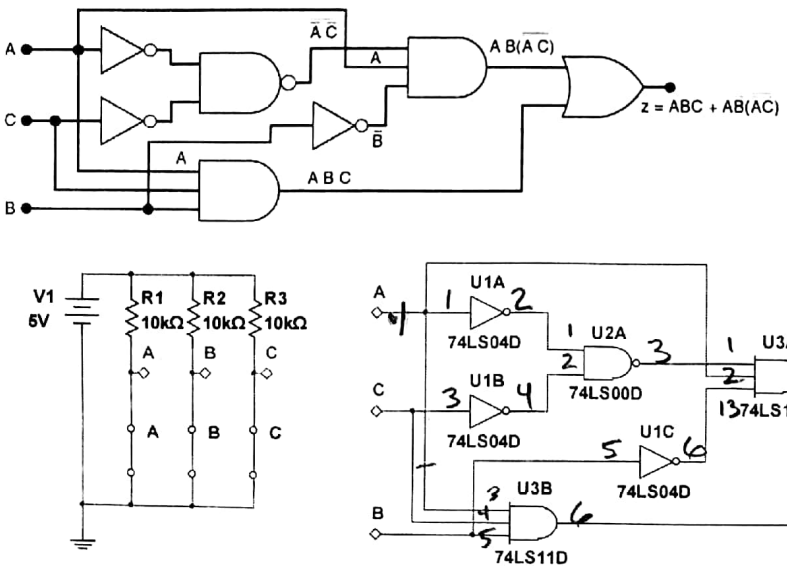


Figure 1- Lab 7 Schematic

$ABC + A\bar{B}(\overline{\bar{A}\bar{C}})$

$ABC + A\bar{B}(\bar{\bar{A}} + \bar{\bar{C}})$

$ABC + A\bar{B}(A + C)$

$ABC + A\bar{B}A + A\bar{B}C$

$ABC + A\bar{B} + A\bar{B}C$

$AC(B + \bar{B}) + A\bar{B}$

$= 1$

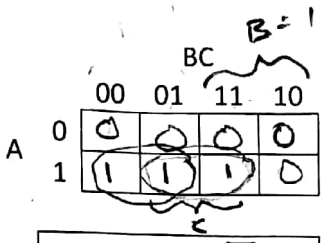
$A \cdot C$

$AC + A\bar{B}$

Simulated			
A	B	C	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Test			
A	B	C	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Table 1 Simulation vs Test



X = $AC + A\overline{B}$ SOP form

X = $A \cdot (C + \overline{B})$ POS form

Table 2 Karnaugh Map of circuit

$AC + A\overline{B}$

Using simulation and test results complete the Karnaugh Map in Table 2 and express the Boolean results in SOP and POS format.

Observations:_____

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Lab 8 – Circuit Reduction (Part 2)

Names: Juddo Abaker, Brett Barnett, Steve Kepler
Date: 10 November 2017

The purpose of this lab is to:
Learn how to reduce a circuit design down to the smallest size using the 17 Theorems and Karnaugh maps. Part 2 will explore how to reduce the circuit. You will also need the results of Lab 7.

Select three 10kohm resistors.
Measure and record the resistance of each resistor.

Equipment needed:

1 – Digital Multimeter
3 – 10Kohm
1 – 4 position dip switch
1 – 74LS04 Hex Inverter
1 – 74LS08 Quad AND
1 – 74LS32 Quad OR

Using Multisim simulate Figure 1 for each input and record in Table 1. Then build and test circuit and record in Table 1

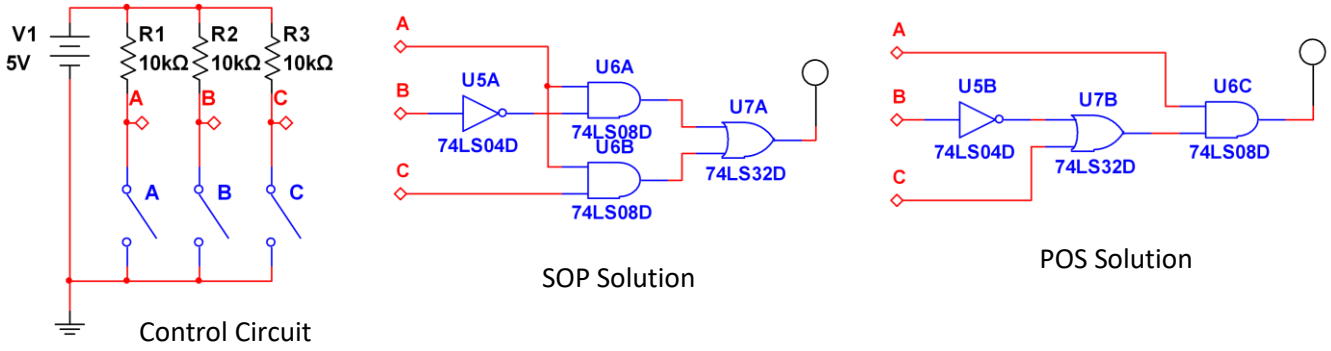

Figure 1- Lab 8 Schematic

Simulated					
				Output	
A	B	C	Lab 7	SOP	POS
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	1	1	1

Test					
				Output	
A	B	C	Lab 7	SOP	POS
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	1	1	1

Table 1 Simulation vs Test

Observations:_____
_____
_____
_____
_____

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Lab 9 – 1 to 3 clock using JK Flip Flops and 555 Timer

Names: STEVE KEPLER, JUDDO ABAKER
Date: 12-1-2017

The purpose of this lab is to:
Many times you can use multiple harmonically related clocks to test a combinational circuits. The Purpose of this lab is to show students how to create a small multiple clock counter circuit that uses JK Flip Flops and a 55 Time

Equipment needed:

1 – 555 Timer
1 – 1Kohm
1 – 4 position dip switch
2 – 74LS73 Dual JK flip flop with clear
2 – Resistors (To Be Designed)
2 – Capacitors (To Be Designed)

Using Multisim simulate design and build a very low frequency clock using a 555 Timer, two resistors and two capacitors. To do this you will need to use the datasheet, Excel and Multisim. Record the component and performance values in Table 1

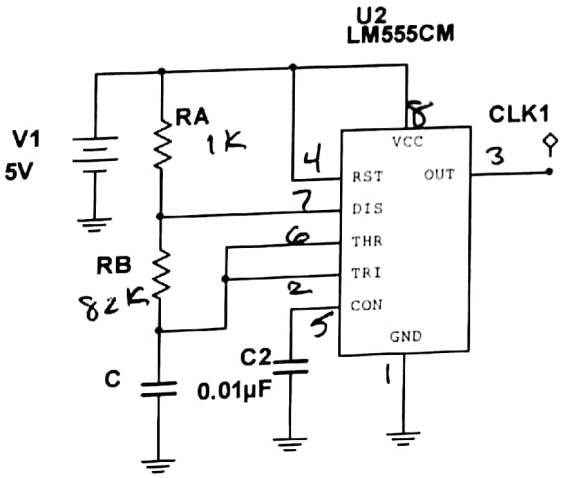


Figure 1 - Lab 9 Astable Oscillator (Clock)

	Designed	Measured
R_A =	1,000 Ω	986.05 Ω
R_B =	82,000 Ω	81,620 Ω
C =	1.00 µF	0.990 µF
t_1 =	0.058 s	0.059 s
t_2 =	0.057 s	0.059 s
T =	0.1151 s	0.1175 s
f =	8.695 Hz	8.511 Hz
f =		
D =	49.7%	50%

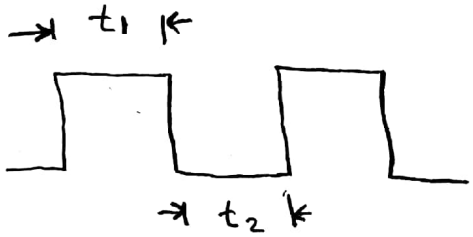


Table 1 Simulation vs Test

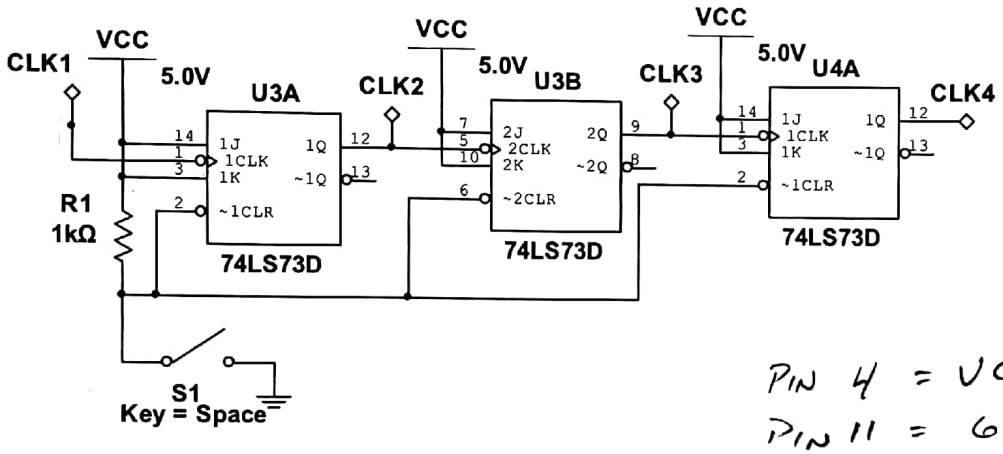
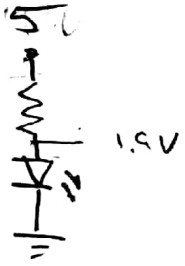


Figure 2 – 3 bit counter using 74LS73s

Verify that there are 3 unique clocks that are harmonically related to CLK1



$V = IR$

$(5 - 1.9)V = 0.016A\,(R)$

$3.1 = 0.016A\,(R)$

$\frac{3.1}{0.016} = 193\,\Omega$

Observations: